



Analog Reinvented

The Sabre ES9822 PRO is the world's highest performance 32-bit analog-to-digital (A/D) converter targeted for professional audio applications such as recording systems, mixer consoles and digital audio workstations (DAW), test equipment, instruments, audio processors, digital turntables, and consumer applications.

The ES9822 PRO has 2 integrated ADCs which use the ESS proprietary 32-Hyperstream II™ ADC Architecture, which delivers unprecedented audio sound quality and specifications, including a DNR of +127dB in mono mode and a DNR of +124dB, THD+N of -117dB in 2 channel mode.

The SABRE ADC supports synchronous SPDIF, I2S master/slave, or native DSD output. For the most demanding audio enthusiast, the ES9822 PRO is capable of outputting RAW data, allowing the user to apply their own custom handling of the data.

The ES9822 PRO comes in a small compact package and consumes less than 170mW.

The ES9822 is able to use preprogrammed filter coefficients to match perfectly with the SABRE PRO Series of DACs including the ES9038PRO. These complimentary filters allow for analog-digital-analog processing with the upmost audio fidelity and minimized time-domain smearing.

The Audio Signal Processor (ASP) integrated in the ADC allows for custom filtering such as RIAA presets to be implemented in the ADC, eliminating the need for re-processing later in the signal path.

The ES9822 PRO has an Ultra-Low Noise Floor Bandwidth of 200kHz. This bandwidth is up to 10 times wider than the competition, enabling higher resolution at higher sample rates.

3

FEATURE	DESCRIPTION
+124dB DNR per channel +127dB DNR in mono mode -117dB THD+N per channel -118dB THD+N in mono mode	Unprecedented dynamic range and ultra-low distortion
High Sample Rates	Up to PCM 768kHz Up to DSD512
Audio Signal Processors (ASP)	Available for custom FIR filters for any applications
Multiple Output formats available	PCM, TDM, DSD, S/PDIF, RAW
Customizable filter characteristics	8 presets, and programmable filter coefficients for custom sound signature 2 audio signal processors for custom filter architectures and analog/digital mixing
I2C or SPI interface control	Configured by microcontroller or other serial interface source
Integrated low noise ADC reference regulators	Reduced BOM cost, PCB area and improved DNR.
Low Power Consumption	Simplifies power supply design
Low Pin Count standardized Packaging	5mm x 5mm, 40 pin QFN
Ultra-Low Noise Floor Bandwidth	200kHz bandwidth enabling higher resolution at higher sample rates

APPLICATIONS

- Professional digital audio workstations Audio Recording
- Very high quality microphones
- High Quality Record Turntable to USB conversion



Functional Block Diagram

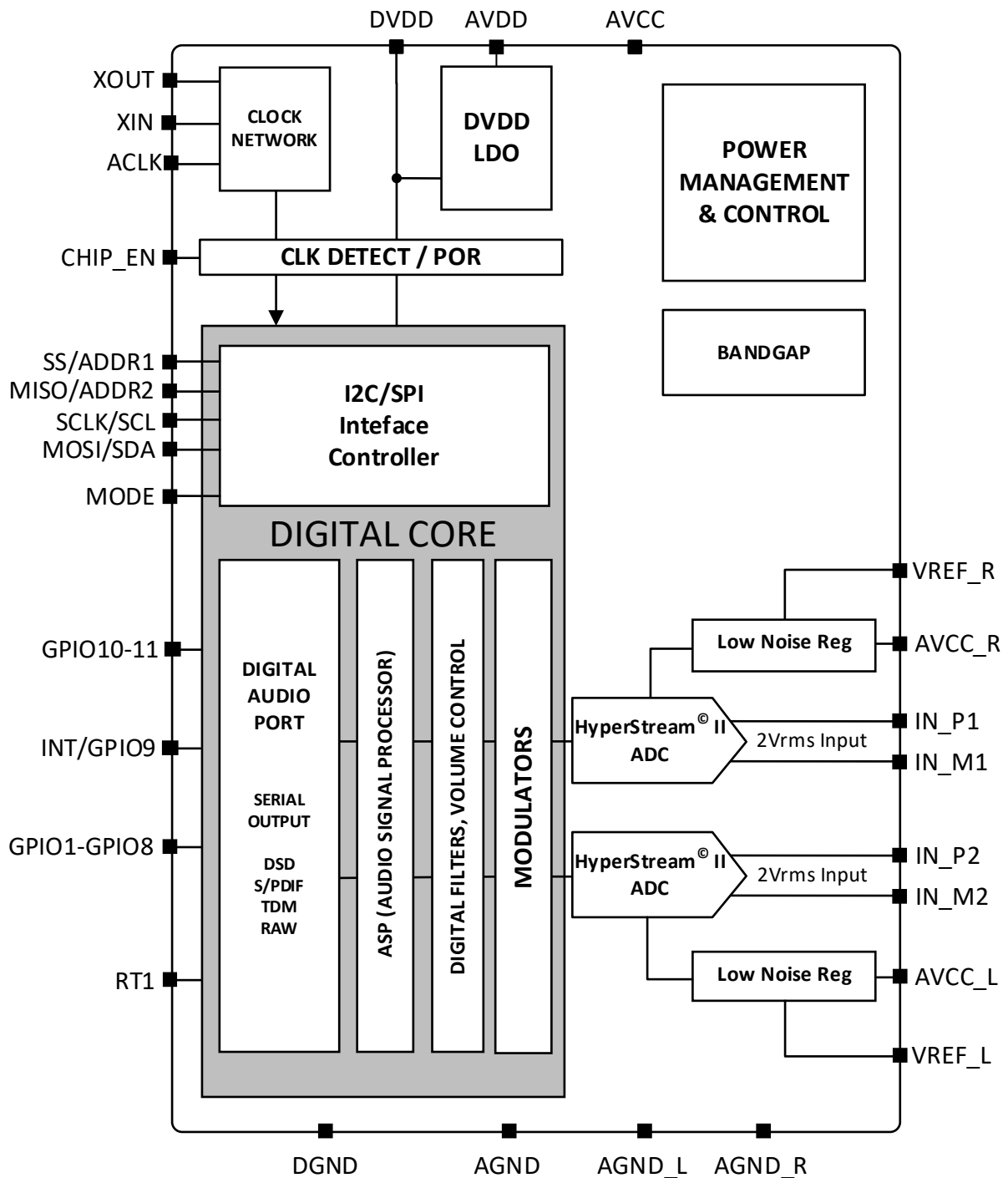
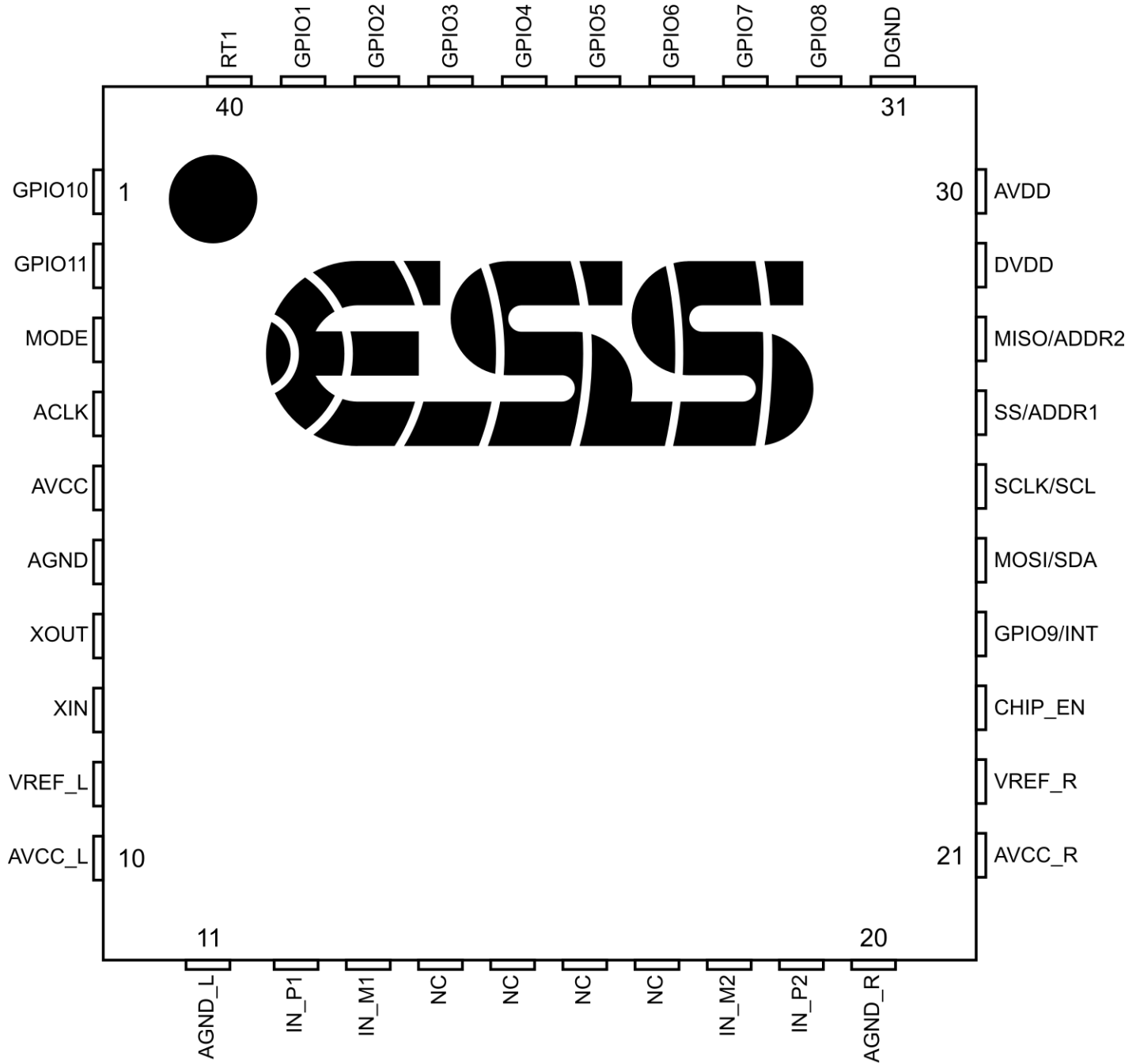


Figure 1. ES9822 PRO Block Diagram



ES9822 PRO Pinout



ES9822Q
(Top View)



40 QFN Pin Descriptions

Pin	Name	Pin Type	Reset State	Pin Description
1	GPIO10	I/O	HiZ	General I/O w/extended functions
2	GPIO11	I/O	HiZ	General I/O w/extended functions
3	MODE	I/O	HiZ	I2C or SPI Control selection
4	ACLK	AI	HiZ	Auxiliary Clock Input
5	AVCC	Power	Power	4.5V Supply
6	AGND	Ground	Ground	Analog Ground
7	XOUT	AO	HiZ	Crystal Output
8	XIN	AI	HiZ	Crystal Input/Oscillator Input
9	VREF_L	Power	Power	Low Noise reference for on-chip regulator, left side
10	AVCC_L	Power	Power	ADC reference voltage (4.5V Supply)
11	AGND_L	Ground	Ground	Analog Ground
12	IN_P1	AI	HiZ	ADC Channel 1 differential positive (+) input
13	IN_M1	AI	HiZ	ADC Channel 1 differential negative (-) input
14	NC	-	-	No Connect
15	NC	-	-	No Connect
16	NC	-	-	No Connect
17	NC	-	-	No Connect
18	IN_M2	AI	HiZ	ADC Channel 2 differential negative (-) input
19	IN_P2	AI	HiZ	ADC Channel 2 differential positive (+) input
20	AGND_R	Ground	Ground	Analog Ground
21	AVCC_R	Power	Power	ADC reference voltage (4.5V Supply)
22	VREF_R	Power	Power	Low Noise reference for on-chip regulator, right side
23	CHIP_EN	I/O	HiZ	Active-high chip enable.
24	GPIO9	I/O	HiZ	General I/O w/extended functions, including INT (INTERRUPT)
25	MOSI/SDA	I/O	HiZ	Serial communication, MOSI(SPI), SDA(I2C), controlled by MODE
26	SCLK/SCL	I/O	HiZ	Serial Clock, SCLK (SPI), SCL (I2C), controlled by MODE
27	SS/ADDR1	I/O	HiZ	I2C Address Select 1, controller by MODE
28	MISO/ADDR2	I/O	HiZ	I2C Address Select 2, controlled by MODE
29	DVDD	Power	Power	Digital Core Supply. Internally Supplied
30	AVDD	Power	Power	3.3V, I/O Supply
31	DGND	Ground	Ground	Digital Core Ground
32	GPIO8	I/O	HiZ	General I/O w/extended functions, Serial Data 8
33	GPIO7	I/O	HiZ	General I/O w/extended functions, Serial Data 7
34	GPIO6	I/O	HiZ	General I/O w/extended functions, Serial Data 6
35	GPIO5	I/O	HiZ	General I/O w/extended functions, Serial Data 5
36	GPIO4	I/O	HiZ	General I/O w/extended functions, Serial Data 4
37	GPIO3	I/O	HiZ	General I/O w/extended functions, Serial Data 3
38	GPIO2	I/O	HiZ	General I/O w/extended functions, Serial Data 2
39	GPIO1	I/O	HiZ	General I/O w/extended functions, Serial Data 1
40	RT1	I	HiZ	Reserved. Must be connected to DGND for normal operation.
41*	Package PAD	-	-	Not electrically connected, used for heat dissipation

* Note: Pin 41 is the package pad.

ES9822 PRO Product Brief



Ordering Information

Part Number	Description	Package
ES9822QPRO	SABRE 32-bit 2 Channel ADC with built in programmable filters, ASPs, and multiple output formats	5mm x 5mm 40 QFN

Revision History

Current Version 0.2.6

Rev.	Date	Notes
0.2.2	Oct 30, 2020	Initial release
0.2.3	Nov 2, 2020	Updates
0.2.4	Nov 6, 2020	Updated Pinout (AVCC naming)
0.2.5	Nov 17, 2020	Updated Pin 28 naming on pinout
0.2.6	Dec 10, 2020	Changed I2C or SPI interface control description on cover page Updated performance data

No part of this publication may be reproduced, stored in a retrieval system, transmitted, or translated in any form or by any means, electronic, mechanical, manual, optical, or otherwise, without the prior written permission of ESS Technology, Inc. ESS Technology, Inc. makes no representations or warranties regarding the content of this document. All specifications are subject to change without prior notice. ESS Technology, Inc. assumes no responsibility for any errors contained herein. U.S. patents pending.