About Jitter:
Digital Audio's weakest link
October 2011
Overview of this Presentation

• What is jitter?
  Why does jitter degrade the perceived audio quality?

• What do Phase Locked Loops do?

  What is an Asynchronous Sample Rate Converter
  and how can that help?
Digital circuit have a clock

- The clock tells the digital circuit when to move on to the next thing, the next sample in a digital audio stream for example

- The edges are supposed to arrive on a very regular schedule: 22.68uS between edges for a CD player
Perfect regularity is impossible

There is variation in the time interval between edges

- All these times should have been 22.68uS, but they are not: some are faster, some are slower
• Interestingly, the DAC appears to get it wrong with jitter. But it's not the wrong value, it's the wrong time...
Clearly we need a low jitter clock to the DAC:

- Low jitter means all the edges are very similar
The system level problem

• We cannot use a very good clock at the DAC
  Because we are not master of the data source!
    – Any clock we use will eventually get out of step with the data
      being sent from the data source, from the CD for example

• Our problem is that there is a “transport clock” that is not
  in our control that is sending the data to us
    – We must remain “locked” to this clock
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Phase Locking solves the problem

- This is the well-known solution
  - A Phase Locked Loop (PLL) at the DAC site “locks” to the incoming data stream and creates the DAC clock that never gets out of step with the transport clock
But the bad news is:

- Audiophiles can hear artifacts from the PLL
  - Hard as it is to believe, it is undoubtedly true: Experiments show that the presence of a PLL is audible – it degrades the audio quality

- Work has focused on how to make the PLL inaudible
  - Audio engineers reduce the phase noise of the PLL
    - Use a crystal-based PLL
    - Use a very high performance loop filter
    - Etc

- Now manufacturers try to remove the PLL completely
  - But they require specialist and non-standard data sources....
Make the DAC Clock the master

- Put the PLL in the data source
  - Now the PLL jitter does not degrade quality at all (even if the jitter in the PLL is high – it does not affect audio quality)
Is there another way to do this?

- PLL in the data source is good, but you have to buy all new data sources (CD, BD, etc)
- And you certainly cannot do USB audio, or Ipod etc

- Recall why the PLL is there:
  - It is needed because our potentially ultra-low noise DAC clock will eventually get out of step with the transport clock
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What is an Asynchronous Sample Rate Converter and how can that help?
• Each day my wife goes to collect the eggs. Our chickens are not “regular” - they do not lay exactly one egg a day, the chicken's egg laying and the days do not remain “locked”: they are asynchronous
These are the eggs we get. Look at the schedule for one chicken: its egg laying and the days get out of sync. Just like the audio problem, sometimes when we want an egg it is not there.

Sometimes, when the DAC wants a new sample, it is not there because the transport clock has not delivered it.

<table>
<thead>
<tr>
<th>Day</th>
<th>Eggs</th>
<th>One Chicken</th>
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<tbody>
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• There is an algorithm, that given the egg schedule 110111101110111011... as collected only at 8:00am, can calculate the very second that the egg is halfway out of the chicken!
  – This means that in principle at least, a digital system operating on its own clock (8.00am each day) asynchronous to the transport clock (the chickens schedule) can figure out exactly when the data should be there (when the egg is coming)
• And this means that in principle we do not need a PLL even though the systems are asynchronous
  – The algorithm to do this is ESS's patented “Asynchronous Sample Rate Convertor” and is not the same as the previously known techniques
Note the ideal aspects:
- The very low noise clock goes straight to the DAC
- The data source has no PLL: existing CD/BD/USB/IPod all work

The “Digitally Recovered Transport Clock” is not a clock!
- It is the egg algorithm running and telling the ASRC exactly where the data should be (when the egg was laid)
What does the ASRC actually do?

• This is the key: what does the ASRC do with the knowledge of where the data “really” is? This is very hard to describe* – but I am going to try
  – Remarkably, as the data flows into the clock domain of DAC the ASRC never actually creates or destroys a sample!
  – It uses the faulty samples in the DAC domain and makes a slight correction to approximately every 600th one that goes past.
  – This is all that needs to be done to remove all artifacts of the asynchronous nature of the transport and DAC clock

*You may wish to read the patents 7,436,333; 7,330,138 and 7,953,782.
No PLL at all

- Using the Sabre DAC clocking scheme the jitter is that of the fixed frequency master DAC oscillator
  - You can buy and use an ultra-high performance clock as designed to RF applications. It far exceeds any PLL
  - That clock can be any frequency at all from about 20-100Mhz
- ►The audio quality suffers no degradation due to PLL artifacts

[ For more technical information from ESS email to wendy.chafer@esstech.com - mention RMAF]
Sabre DAC: Conclusions

- ESS delivers to the Audiophile community the best DAC and ADC silicon chips.
- The top of the line “Sabre” products include
  - HyperStream: DACs and ADCs to true Audiophile levels without the problems of ΣΔ artifacts
  - ASRC technology: removes jitter from the signal source without introducing PLL artifacts
  - The best digital volume controls (in both DAC and ADC)
  - More we have not spoken about today, optimized DEM, lowest power, least susceptibility to EMI, lowest out of band noise, built in SPDIF, built in SADC, 8/4/2/1 channels ... etc etc

Martin Mallinson ESS, 2011 RMAF
End of Presentation

Thank you for attending