Analog Reinvented

ES9841

4 Channel High Performance ADC

Product Datasheet

The SABRE ES9841 is a synchronous, high-performance 4-channel analog-to-digital (ADC) converter that targets professional and consumer applications with outstanding audio quality and low bill-of-materials.

The ES9841 incorporates 4 ADCs using ESS' patented Hyperstream® IV architecture which delivers unprecedented audio sound quality and specification of a True DNR of +122dB and a THD+N of -115dB per channel in 4 channel mode and a True DNR of +125dB in stereo mode.

The SABRE® ADC supports S/PDIF encoding, I²S master/slave, TDM outputs and PDM microphone inputs. The ES9841 can be controlled by software (I²C /SPI slave) or hardware mode (HW) to reduce programming complexity. A Master SPI port is also integrated allowing for external control of other devices.

The ES9841 has an integrated patented Analog PLL which eliminates the requirement for an external oscillator with no loss in specified performance.

Built-in pre-programmed digital filters, including a DC blocking filter, allowing for custom sound and latency preferences.

The ES9841 has an Ultra-Low Noise Floor Bandwidth of 200kHz. This bandwidth is up to 10 times wider than the competition, enabling higher resolution at higher sample rates.

The ES9841 sets the standard for recording capabilities with regards to audio performance and customization, in a form factor that is required for the most demanding recording applications.

FEATURE	DESCRIPTION
+122dB True DNR per channel +125dB True DNR 2 channel mode -115dB THD+N ratio per channel	Very high dynamic range with ultra-low noise and distortion
High Sample Rates	Support for sample rates up to and including 768kHz (using 64FS mode)
Integrated Analog PLL	Improved low jitter Analog PLL to generate clocks and optionally eliminate the need for external oscillator with no performance loss
Integrated Low Noise ADC Reference Regulators	Reduces BOM cost and printed circuit board (PCB) area
S/PDIF Encoding	Integrated PCM data to S/PDIF output format
Customizable Filter Selection	8 preset digital optimal filters + a DC blocking filter
I²C, SPI & Hardware Control Interface	Standard I²C or SPI interface for programming registers, or by bootstrapping pins in Hardware (HW) mode
Multiple Output Formats	Supports Serial Data Interface including TDM, I²S, LJ and S/PDIF outputs
Low Power Consumption (mW/Ch)	Simplifies Power Supply Design
Low Pin Count Standardized Packages	5mm x 5mm, 40 pin QFN, drop-in compatible with ES9840 (See pinout)

APPLICATIONS

- Professional DAW Audio Recording
- Very high-quality microphones
- High quality record turntable to USB conversion
- Professional Audio Equipment

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Functional Block Diagram

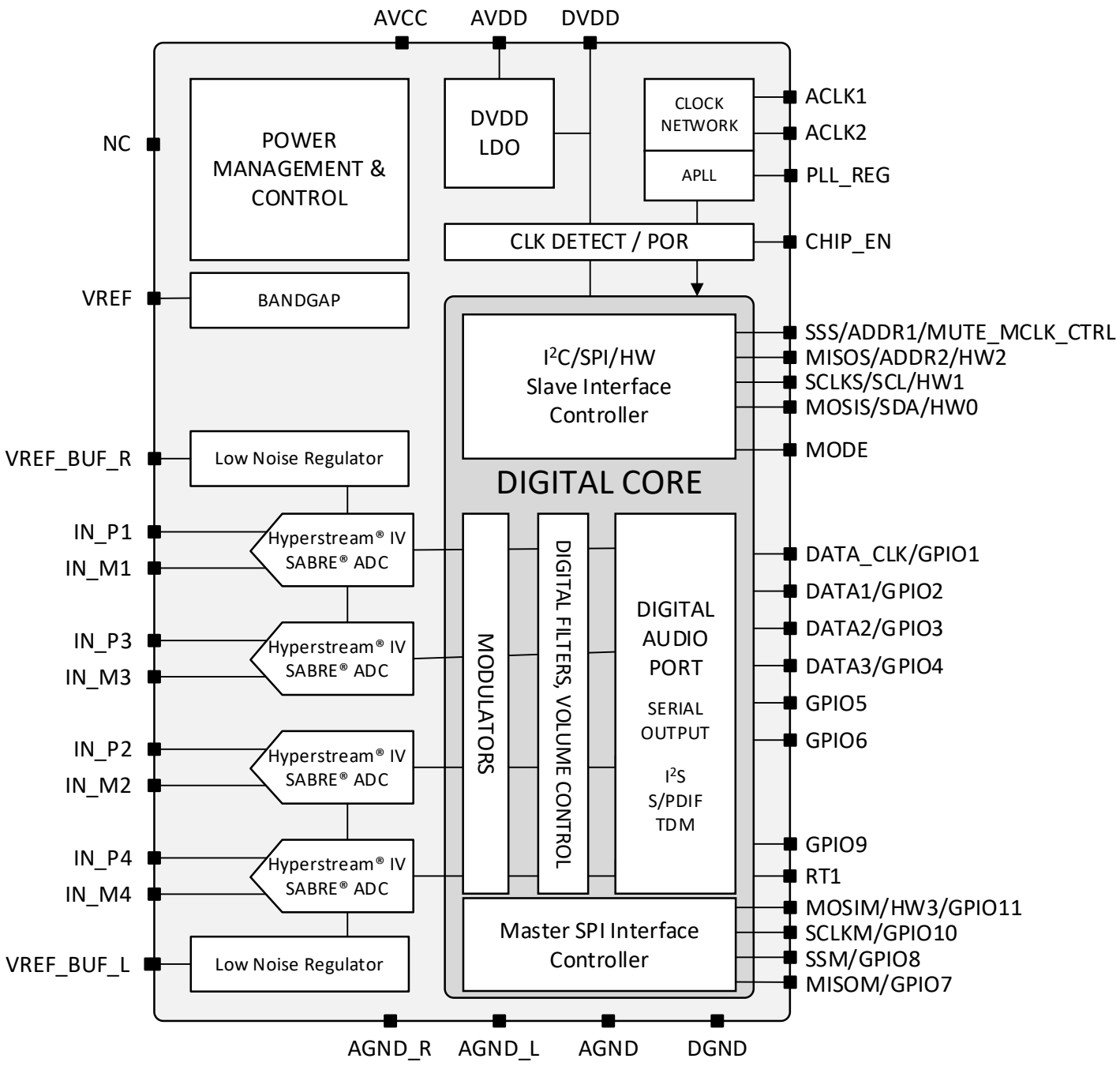


Figure 1 - ES9841 Block Diagram

ES9841 Package

40 QFN Pinout

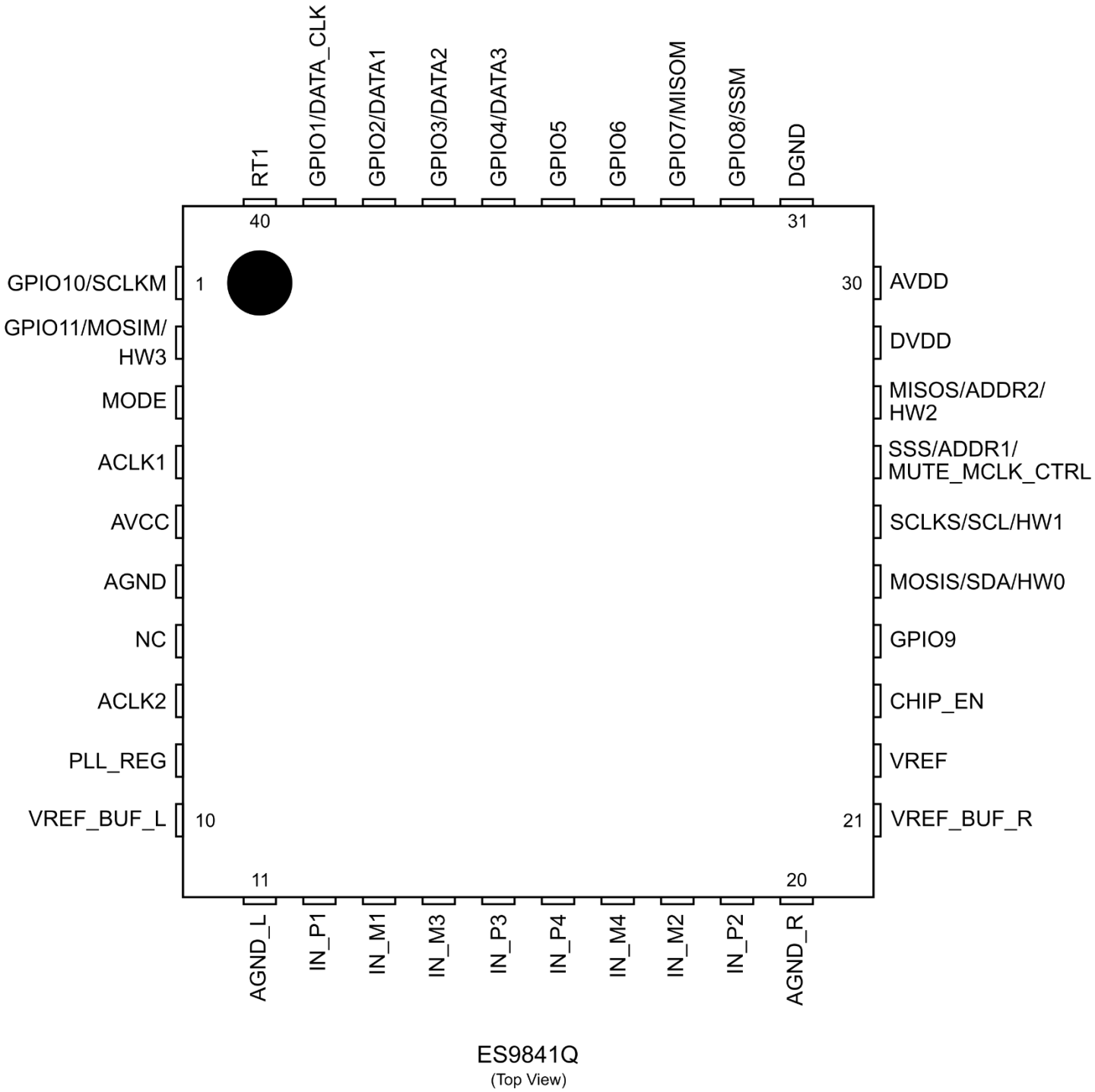


Figure 2 - ES9841 Pinout

40 QFN Pin Descriptions

Pin	Name	Pin Type	Reset State	Pin Description
1	GPIO10	D I/O	HiZ	General I/O 10
	SCLKM			SPI Serial Clock pin (Master), controlled by MODE
2	GPIO11	D I/O	HiZ	General I/O 11
	MOSIM			SPI Main Out Sub In pin (Master), controlled by MODE
	HW3			Hardware 3 interface pin, controlled by MODE
3	MODE	D I/O	HiZ	I²C/SPI Control selection or HW mode
4	ACLK1	Clock I	HiZ	Clock Input 1
5	AVCC	Power	Power	Analog Supply
6	AGND	Ground	Ground	Analog Ground
7	NC	-	-	No Connect
8	ACLK2	Clock I	HiZ	Clock Input 2
9	PLL_REG	A O	P/D	Low Noise Supply for PLL. Internally generated. Requires an external 1µF decoupling capacitor to ground. See Reference Schematic for details
10	VREF_BUF_L	A O	P/D	Left Low Noise Supply for ADC. Internally generated. Requires an external 1µF decoupling capacitor with low ESR to ground and an external 100nF decoupling capacitor to ground. See Reference Schematic for details
11	AGND_L	Ground	Ground	Analog Ground Left
12	IN_P1	A I	HiZ	ADC Channel 1 differential positive (+) input
13	IN_M1	A I	HiZ	ADC Channel 1 differential negative (-) input
14	IN_M3	A I	HiZ	ADC Channel 3 differential negative (-) input
15	IN_P3	A I	HiZ	ADC Channel 3 differential positive (+) input
16	IN_P4	A I	HiZ	ADC Channel 4 differential positive (+) input
17	IN_M4	A I	HiZ	ADC Channel 4 differential negative (-) input
18	IN_M2	A I	HiZ	ADC Channel 2 differential negative (-) input
19	IN_P2	A I	HiZ	ADC Channel 2 differential positive (+) input
20	AGND_R	Ground	Ground	Analog Ground Right
21	VREF_BUF_R	A O	P/D	Right Low Noise Supply for ADC. Internally generated. Requires an external 1µF decoupling capacitor with low ESR to ground and an external 100nF decoupling capacitor to ground. See Reference Schematic for details
22	VREF	A O	P/D	Low Noise Supply. Internally generated. Requires an external 1µF decoupling capacitor to ground.

				See Reference Schematic for details
23	CHIP_EN	Reset	HiZ	Active-high chip enable.
24	GPIO9	D I/O	HiZ	General I/O w/extended functions
25	MOSIS	D I/O	HiZ	SPI Main Out Sub In pin (Slave), controlled by MODE
	SDA			I²C Serial Data pin, controlled by MODE
	HW0			Hardware 0 interface pin, controlled by MODE
26	SCLKS	D I/O	HiZ	SPI Serial Clock pin (Slave), controlled by MODE
	SCL			I²C Serial Clock pin, controlled by MODE
	HW1			Hardware 1 interface pin, controlled by MODE
27	SSS	D I/O	HiZ	SPI Slave Select (Slave) pin, controlled by MODE
	ADDR1			I²C Address 1 pin, controlled by MODE
	MUTE_MCLK_CTRL			Hardware Mute Control pin, controlled by MODE
28	MISOS	D I/O	HiZ	SPI Main In Sub Out pin (Slave), controlled by MODE
	ADDR2			I²C Address 2 pin, controlled by MODE
	HW2			Hardware 2 interface pin, controlled by MODE
29	DVDD	A O	P/D	Digital Core Supply. Internally generated. Requires an external 1µF decoupling capacitor to ground. See Reference Schematic for details
30	AVDD	Power	Power	Digital & I/O Supply
31	DGND	Ground	Ground	Digital Core Ground
32	GPIO8	D I/O	HiZ	General I/O 8 w/extended functions
	SSM			SPI Slave Select (Master) pin, controlled by MODE
33	GPIO7	D I/O	HiZ	General I/O 7 w/extended functions
	MISOM			SPI Main In Sub Out pin (Master), controlled by MODE
34	GPIO6	D I/O	HiZ	General I/O 6 w/extended functions
35	GPIO5	D I/O	HiZ	General I/O 5 w/extended functions
36	GPIO4	D I/O	HiZ	General I/O 4 w/extended functions
	DATA3			Serial Data 3
37	GPIO3	D I/O	HiZ	General I/O 3 w/extended functions
	DATA2			Serial Data 2
38	GPIO2	D I/O	HiZ	General I/O 2 w/extended functions
	DATA1			Serial Data 1
39	GPIO1	D I/O	HiZ	General I/O 1 w/extended functions
	DATA_CLK			Serial Data clock
40	RT1	D I	HiZ	Reserved. Must be connected to DGND for normal operation.

41	Package Pad[1]	-	-	Not electrically connected, used for heat dissipation. Connect to DGND

Table 1 - ES9841 40 QFN Pin Descriptions

[1] Pin 41 is the package pad. See 40 QFN package dimensions for sizing. Connect to DGND.

Feature List

The ES9841 has an extensive feature list. When compared to the previous generation ES9840, the ES9841 has added:

- The ES9841 has a True DNR of +122dB
- Integrated Analog PLL and low noise analog regulators
- Individual digital gain settings for each channel of 0 to +42dB in +6dB steps
- Hyperstream® IV Architecture improves audio performance while consuming less power than previous generations.
- Improved THD+N linearity
- Hardware Modes
- SPI Master Interface
- ADC Clipping GPIO output

Configuration Modes

The ES9841 has 4 control programming modes which are controlled by the state of the MODE pin (Pin 3).

MODE PIN	Configuration
0	I²C Interface
Pull 0	HW control mode (see Hardware Mode Table)
Pull 1	HW control mode (see Hardware Mode Table)
1	SPI Interface

Table 2 - Mode Pin Configuration Options

Design Information

Hardware pins can be configured in 4 different ways. Each pin can be tied-high (1), pulled-high (Pull 1), pulled-low (Pull 0), or tied-low (0). HW0 and HW1 pins are always tied-high or tied-low. These 4 options also apply to MUTE_MCLK_CTRL.

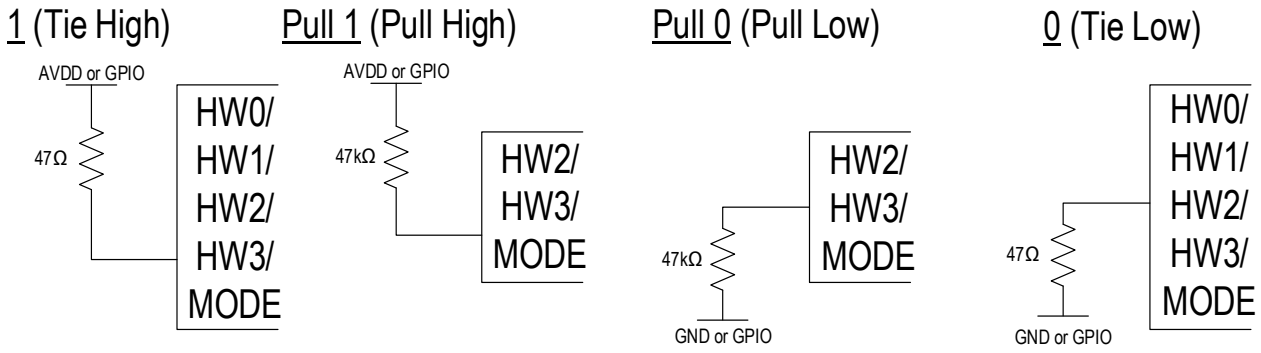


Figure 3 - Example Hardware Mode Pin Configurations

Software Mode

The ES9841 supports a slave I²C or SPI serial communication in software mode. There are two types of registers, read/write registers and read-only registers. Software modes are set when the MODE pin is a 0 (0V) for I²C or a 1 (AVDD) for SPI.

A system clock is not required to read and write registers.

I²C Slave Interface Commands

- MODE (Pin 3) – 0 (Tied-Low)
- Connect per I²C standard
  - SDA (Pin 25)
  - SCL (Pin 26)
  - ADDR1 (Pin 27)
  - ADDR2 (Pin 28)

I²C Address	ADDR2	ADDR1
0x40	GND	GND
0x42	GND	AVDD
0x44	AVDD	GND
0x46	AVDD	AVDD

Table 3 - I²C Addresses

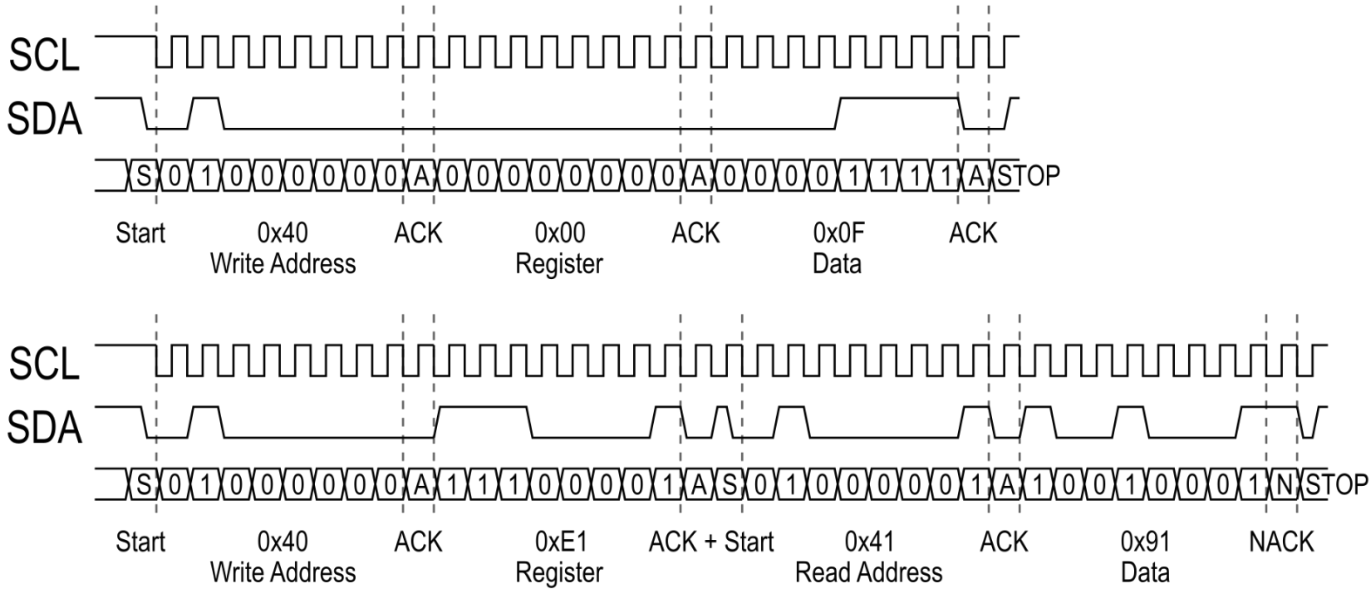


Figure 4 - I²C Write and Read Example

Note: CHIP_ID for the ES9841 is 0x91 in Register 225 (0xE1)

SPI Slave Interface Commands

- MODE (Pin 3) – 1 (Tied-High)
- Connect per SPI standard
  - MOSIS (Pin 25)
  - SCLKS (Pin 26)
  - SSS (Pin 27)
  - MISOS (Pin 28)

SPI Command	First Byte
Write	0x03
Read	0x01

Table 4 - SPI Commands

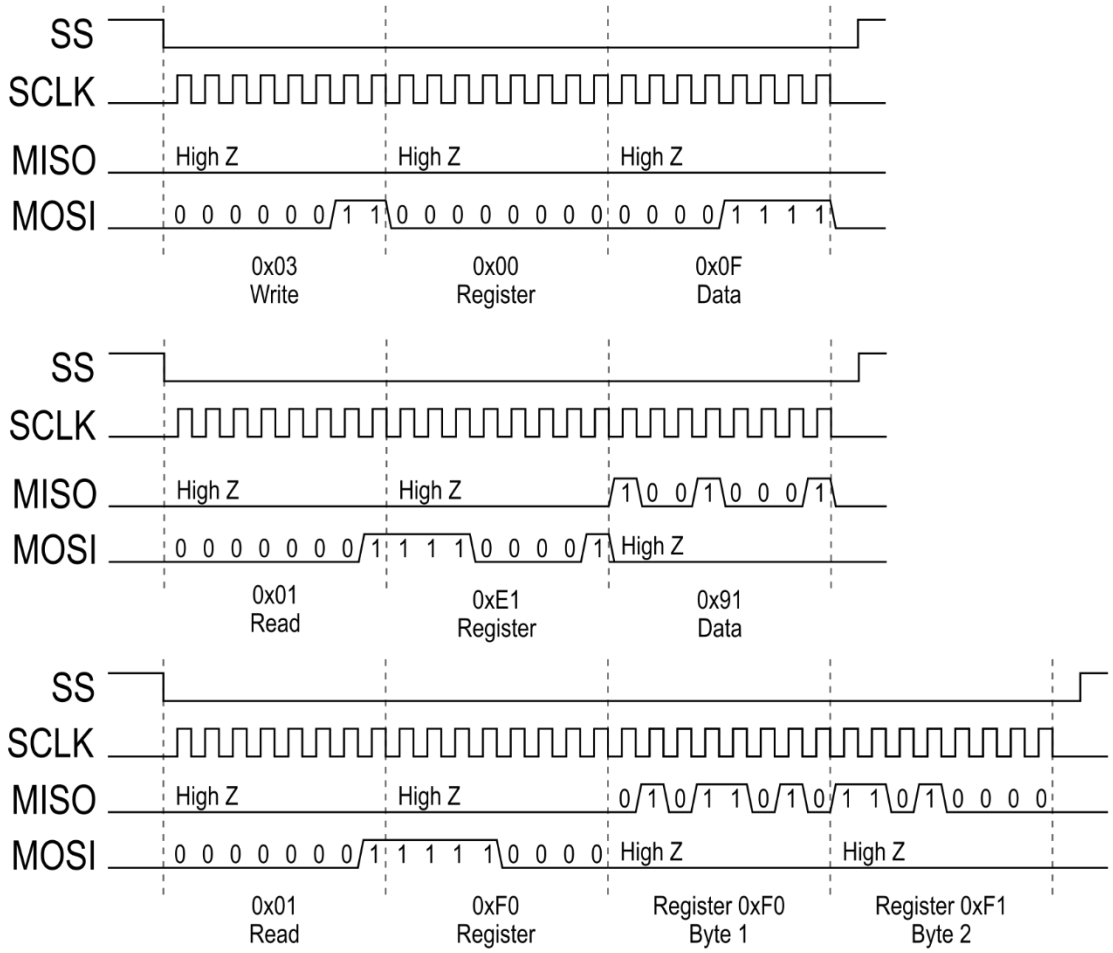


Figure 5 - SPI Write, Read, and Multi-byte Read Example

Note: CHIP_ID is 0x91 (ES9841) in Register 225 (0xE1)

MCLK Control

In Software Modes, Register 5[4] - MCLK_24M_DIV2 must be set correctly according to the external MCLK being used.

MCLK_24M_DIV2	MCLK
0	24.576MHz/22.5792MHz
1	49.152MHz/45.1584MHz

Table 5 - MCLK Control in Software Mode

Hardware Mode

The ES9841 has pre-configured hardware modes that can be set with an external pin configuration. These modes configure the ADC for different output formats such as PCM in slave or master mode, or PDM, or configure the ADC in TDM slave modes to combine multiple chips together creating up to 16 channels of digital outputs.

Each hardware mode pin has 4 states that need to be set for each mode according to the Hardware Mode Pin Configurations. Information on how to set the pin to the correct state be found in Table 2 - Mode Pin Configuration Options

Design Information.

These modes are set with pins:

- MODE (Pin 3)
- HW0 (Pin 25)
- HW1 (Pin 26)
- HW2 (Pin 27)
- MUTE_CTRL (Pin 28)

Recommended Hardware Mode Setup Sequence

The Hardware Mode setup sequence is shown below with all hardware pins being defined after CHIP_EN is asserted.

Note: MUTE_CTRL should be set to muted until the HW mode is finalized and after CHIP_EN is asserted, then it may be set to the correct clock rate and unmuted last. See Mute and MCLK Control for more information.

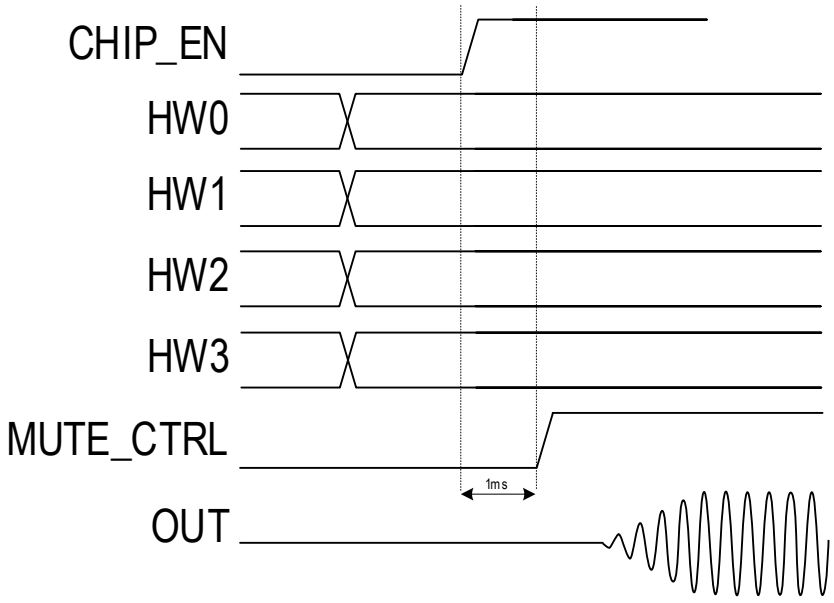


Figure 6 - Hardware Mode Startup Sequence

Hardware Mode Pin Configurations

HW #	Mode Description	FS [kHz]	BCK [MHz]	BCK/Channel	Channel Slots	MCLK [MHz]	Mode	HW2	HW1	HW0
32-bit PCM/SPDIF Master Modes										
0	I²S Master or S/PDIF	MCLK/128	MCLK/2 (64*FS)	32	1, 2 or Mono	128*FS	Pull 0	0	0	0
1	I²S Master or S/PDIF	MCLK/256	MCLK/4 (64*FS)	32	1, 2 or Mono	256*FS	Pull 0	0	0	1
2	I²S Master or S/PDIF	MCLK/512	MCLK/8 (64*FS)	32	1, 2 or Mono	512*FS	Pull 0	0	1	0
3	I²S Master or S/PDIF	MCLK/1024	MCLK/16 (64*FS)	32	1, 2 or Mono	1024*FS	Pull 0	0	1	1
4	LJ Master or S/PDIF	MCLK/128	MCLK/2 (64*FS)	32	1, 2 or Mono	128*FS	Pull 0	Pull 0	0	0
5	LJ Master or S/PDIF	MCLK/256	MCLK/4 (64*FS)	32	1, 2 or Mono	256*FS	Pull 0	Pull 0	0	1
6	LJ Master or S/PDIF	MCLK/512	MCLK/8 (64*FS)	32	1, 2 or Mono	512*FS	Pull 0	Pull 0	1	0
7	LJ Master or S/PDIF	MCLK/1024	MCLK/16 (64*FS)	32	1, 2 or Mono	1024*FS	Pull 0	Pull 0	1	1
32-bit PCM/SPDIF Slave, Auto FS Detect & PLL										
8	I²S Slave, Auto FS	8 ≤ FS ≤ 384	64*FS	32	1, 2 or Mono	22.5792 / 24.576 45.1584 / 49.152	Pull 0	Pull 1	0	0
9	I²S Slave, PLL MCLK	48	3.072	32	1, 2 or Mono	45.1584 / 49.152 From PLL[1]	Pull 0	Pull 1	0	1
10	I²S Slave, PLL MCLK	96	6.144	32	1, 2 or Mono		Pull 0	Pull 1	1	0
11	I²S Slave, PLL MCLK	192	12.288	32	1, 2 or Mono		Pull 0	Pull 1	1	1
12	LJ Slave, Auto FS	8 ≤ FS ≤ 384	64*FS	32	1, 2 or Mono	22.5792 / 24.576 45.1584 / 49.152	Pull 0	1	0	0
13	LJ Slave, PLL MCLK	48	3.072	32	1, 2 or Mono	45.1584 / 49.152 From PLL[11]	Pull 0	1	0	1
14	LJ Slave, PLL MCLK	96	6.144	32	1, 2 or Mono		Pull 0	1	1	0
15	LJ Slave, PLL MCLK	192	12.288	32	1, 2 or Mono		Pull 0	1	1	1

Table 6 - Hardware Mode Pin Configurations

[1] Ensure MUTE_CTRL pin (Pin 28) is set to Pull 0 or Pull 1.

Hardware Mode Pin Configurations (Continued)

HW #	Mode Description	FS [kHz]	BCK [MHz]	BCK/Channel	Channel Slots	MCLK [MHz]	Mode	HW2	HW1	HW0
32-bit TDM LJ Slave Modes, Auto FS Detect, Auto CH Num, Toggle Daisy Chain										
16	32-bit TDM LJ Slave Auto FS Auto CH Num	8 ≤ FS ≤ 384	Auto(128FS, 256FS, 512FS, 1024FS)	32	1 to 4	22.5792 / 24.576 45.1584 / 49.152	Pull 1	0	0	0
17		8 ≤ FS ≤ 192	Auto(256FS, 512FS, 1024FS)	32	5 to 8		Pull 1	0	0	1
18		8 ≤ FS ≤ 96	Auto(512FS, 1024FS)	32	9 to 12		Pull 1	0	1	0
19		8 ≤ FS ≤ 96	Auto(512FS, 1024FS)	32	13 to 16		Pull 1	0	1	1
20		8 ≤ FS ≤ 48	Auto(1024FS)	32	17 to 20		Pull 1	Pull 0	0	0
21		8 ≤ FS ≤ 48	Auto(1024FS)	32	21 to 24		Pull 1	Pull 0	0	1
22		8 ≤ FS ≤ 48	Auto(1024FS)	32	25 to 28		Pull 1	Pull 0	1	0
23		8 ≤ FS ≤ 48	Auto(1024FS)	32	29 to 32		Pull 1	Pull 0	1	1
16-bit TDM LJ Slave Modes, Auto FS Detect, Auto CH Num, Toggle Daisy Chain										
24	16-bit TDM LJ Slave Auto FS Auto CH Num	8 ≤ FS ≤ 384	Auto(64FS, 128FS, 256FS, 512FS)	16	1 to 4	22.5792 / 24.576 45.1584 / 49.152	Pull 1	Pull 1	0	0
25		8 ≤ FS ≤ 192	Auto(128FS, 256FS, 512FS)	16	5 to 8		Pull 1	Pull 1	0	1
26		8 ≤ FS ≤ 96	Auto(256FS, 512FS)	16	9 to 12		Pull 1	Pull 1	1	0
27		8 ≤ FS ≤ 96	Auto(256FS, 512FS)	16	13 to 16		Pull 1	Pull 1	1	1
28		8 ≤ FS ≤ 48	Auto(512FS)	16	17 to 20		Pull 1	1	0	0
29		8 ≤ FS ≤ 48	Auto(512FS)	16	21 to 24		Pull 1	1	0	1
30		8 ≤ FS ≤ 48	Auto(512FS)	16	25 to 28		Pull 1	1	1	0
31		8 ≤ FS ≤ 48	Auto(512FS)	16	29 to 32		Pull 1	1	1	1

Table 7 - Hardware Mode Pin Configurations Pt2

GPIO Functions in Hardware Mode

The ES9841 supports specific functions using GPIO pins in hardware mode. The tables below show the available options including ADC Input/Output Select, Automute, Filter Select, Daisy Chain Enable, and Mono Slot Select.

The HW3 Pin is used to select the Input and Output formats of the ADC in hardware mode. HW3 Selects between Analog and PDM Inputs as well as toggles the SPDIF output.

HW3	Input Format	Output Format	Supported HW Modes
0	Analog	I²S/LJ Master	0 - 7
		I²S/LJ Slave	8 - 15
		TDM Slave	16 - 31
Pull 0		S/PDIF	0 - 7
Pull 1	PDM	I²S/LJ Master	0 - 7
		I²S/LJ Slave	8 - 15
		TDM Slave	16 - 31
1		S/PDIF	0 - 7

Table 8 - ADC Input/Output Select with HW3 in Hardware Mode

GPIO8 Function	Supported HW Modes	HW3 Conditions	Function Description
S/PDIF Channel Select	0 - 7	Pull 0, 1 (S/PDIF)	GPIO8 = AVDD – Ch1/2 GPIO8 = GND – Ch3/4
Mono Mode Enable	0 - 15	0 (I²S, LJ Master/Slave)	GPIO8 = AVDD – Mono On GPIO8 = GND – Mono Off
Daisy Chain Enable	16 - 31	0, Pull 1 (TDM Slave)	GPIO8 = AVDD – Not Enabled GPIO8 = GND – Daisy Chain Enabled

Table 9 - GPIO8 Functions in Hardware Mode

GPIO9 Function	Supported HW Modes	HW3 Conditions	GPIO 8 Conditions	Function Description
Stereo Mode Enable	0 - 15	0, Pull 0 (Analog Input)	-	GPIO9 = AVDD – Stereo On GPIO9 = GND – Stereo Off
Mono Slot Select	0 - 15	0 (I²S, LJ Master/Slave)	AVDD (Mono On)	GPIO9 = AVDD – Slot 1 GPIO9 = GND – Slot 2
PDM Clock	All	Pull 1, 1 (PDM Input)	-	PCM CLK [O]

Table 10 - GPIO9 Functions in Hardware Mode

GPIO6 Function	GPIO5 Function	Supported HW Modes	HW3 Conditions	Function Description
{GPIO6, GPIO5} = 2'b00		0-15	0, Pull 0 (Analog Input)	+0dB Digital Gain
{GPIO6, GPIO5} = 2'b01				+18dB Digital Gain
{GPIO6, GPIO5} = 2'b10				+24dB Digital Gain
{GPIO6, GPIO5} = 2'b11				+30dB Digital Gain
PDM Data 2	PDM Data 1	All	Pull 1, 1 (PDM Input)	PDM_DATA1/2 [I]

Table 11 - GPIO 5 & 6 Functions in Hardware Mode

GPIO7	Supported HW Modes	Filter
1'b0	All	Filter 0 Minimum Phase
1'b1		Filter 2 Linear Phase Fast Roll-Off

Table 12 - ADC Filter Select with GPIO7 in Hardware Mode

GPIO10	Supported HW Modes	DC Block
1'b0	All	Disabled
1'b1		Enabled

Table 13 - DC Block Enable with GPIO10 in Hardware Mode

Mute and MCLK Control

Set MUTE_MCLK_CTRL (Pin 27) to mute the output while in Hardware Mode:

HW MUTE Control (Pin 27)	Condition	MCLK [MHz]
0	Mute	22.5792 / 24.576
1	Unmute	22.5792 / 24.576
Pull 0	Mute	45.1584 / 49.152
Pull 1	Unmute	45.1584 / 49.152

Table 14 - Mute and MCLK Control in Hardware Mode

Note: If MUTE_MCLK_CTRL (Pin 27) is set to the incorrect MCLK rate, the ADC may have degraded output performance.

Note: If using the MCLK from PLL Hardware Modes (9-11, 13-15), MUTE_MCLK_CTRL must be set to Pull 0 or Pull 1.

Digital Features

Audio Input/Output Formats

The ES9841 supports multiple serial input/output formats which can be set either through Hardware Mode or Software Mode.

The ES9841 can automatically adjust to the input sample rate in slave modes by enabling Register 1[0] AUTO_FS_DETECT. The output data format is selected using Register 3[6:4] OUTPUT_SEL.

The formats include:

- PCM
  - Slave and master mode in 16, 24, 32 - bit widths
  - I²S and Left-Justified (LJ)
  - Sample rates up to 768kHz (64fs mode)
  - Channel mapping
- TDM
  - Up to 32 slots including daisy chain mode
  - Daisy chain support
  - Slave mode in hardware mode. Slave and master modes in software mode
  - LJ format in hardware modes. I²S or LJ in software modes
  - Channel mapping
- S/PDIF
  - Stereo 2 Channel auxiliary output
  - Channel Pair Select
  - Sample rates up to 192kHz
- PDM Microphone Input
  - Master mode in hardware and software mode
  - Sample rates from PDM64 to PDM512

PCM/TDM Encoder

The ES9841 integrates a 4 Channel 4 Line PCM/TDM Encoder output with a maximum word width of 32-bits (default) and a maximum bit depth of 32-bit (default). The encoder allows for I²S, LJ, and TDM output streams.

The PCM/TDM encoder can support up to 32 different slots and each channel of the ADC can be mapped to any of the 32 slots.

PCM/TDM Encoder/Decoder Registers

- Register 2[0] ENABLE_TDM_ENCODE
- Register 3[6:4] OUTPUT_SEL = 3'b0
- Register 9[6] AUTO_CH_DETECT
- Register 9[4:0] TDM_CH_NUM
- Register 10[5:4] TDM_WORD_WIDTH
- Register 10[3:2] TDM_BIT_WIDTH
- Register 10[1] TDM_VALID_EDGE
- Register 10[0] TDM_LJ
- Register 10[6] NOISE_FLOOR_SHAPE_16BIT

PCM/TDM Encoder Mapping Registers

- Register 11-14[6:5] TDM_ENC_LINE_SEL_CHx
- Register 11-14[4:0] TDM_ENC_SLOT_SEL_CHx

TDM Daisy Chain Registers

- Register 15[7] TDM_ENC_DAISY_CHAIN
- Register 15[4:0] TDM_ENC_DATA_LATCH_ADJ

PCM (I²S, LJ) Format

The input data is organized into 2 channels per data line, up to 2 data lines. Each encoder data slot can be mapped to any ADC channel using Registers 11-14[4:0] TDM_ENC_SLOT_SEL_CHx respectively.

Pin Name	Function	Description
DATA_CLK	PCM BCLK	PCM Clock (Bit Clock), Master or Slave
DATA1	PCM WS	PCM WS (Word Select/Frame Select), Master or Slave
DATA2	PCM ENC DATA1	PCM Encoder Data Channel 1 & 2 (default)
DATA3	PCM ENC DATA2	PCM Encoder Data Channel 3 & 4 (default)

Table 15 - PCM Pin Connections

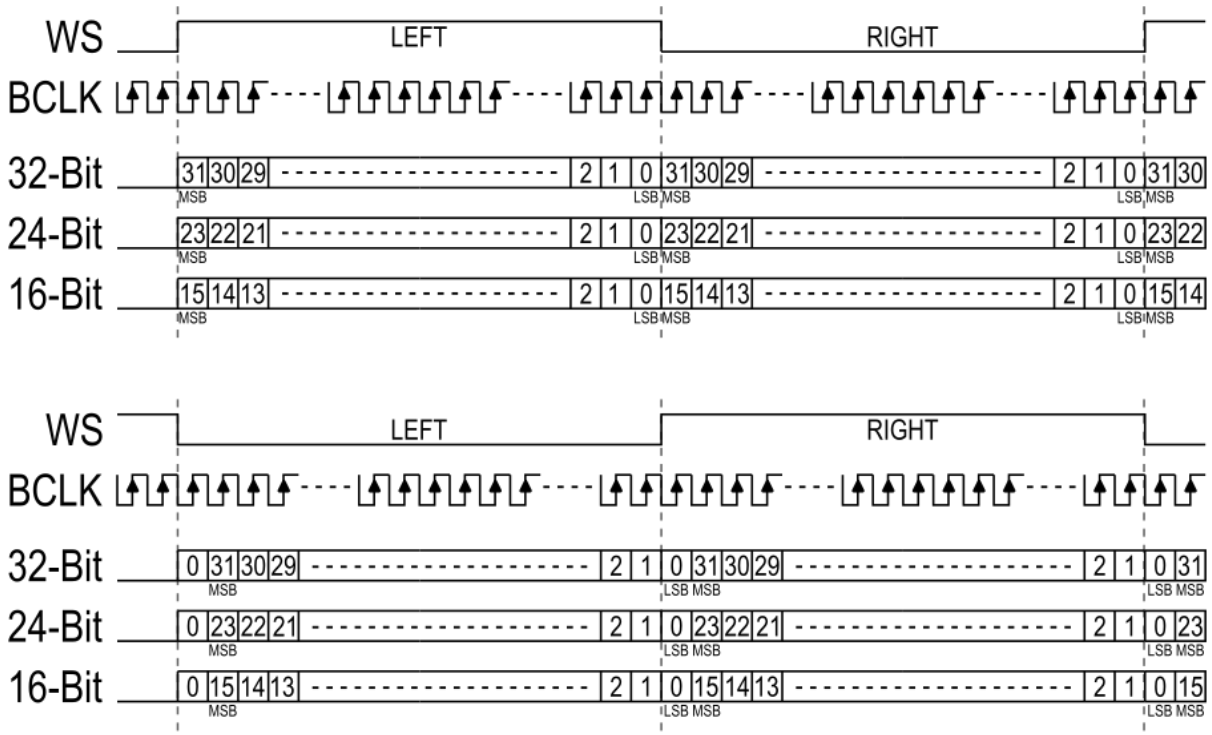


Figure 7 - LJ (top) & I²S (bottom) for 16,24, and 32-bit Word Widths

TDM Format

The ES9841 supports TDM format, allowing for 2 to 32 channels on a single data line. TDM is supported in both software and hardware modes with the 4 Channel 4 Line TDM Encoder supporting outputs through DATA2-5.

In software mode, each encoder data slot can be mapped to any ADC channel using Register 11-14[4:0] TDM_ENC_SLOT_SEL_CHx respectively.

Hardware modes each have their own slots that the four audio channels maps to. For example, in the case of TDM32 (32CH), the hardware mode will be configured so that slots 1 through 4 will map to one device (HW mode #16), slots 5 through 8 will map to a second device (HW mode #17), slots 9 through 12 will map to a third device (HW mode #18), and so on until slots 29 through 32 mapping to a 8th device respectively (HW mode #23).

Pin Name	Function	Direction	Description
DATA_CLK	TDM BCLK	[I/O]	TDM Clock, Master, or Slave
DATA1	TDM WS	[I/O]	TDM WS (Word Select/Frame Select), Master or Slave
DATA2	TDM ENC DATA1	[O]	TDM Encoder DATA1 Channel 1 & 2 (default)
DATA3	TDM ENC DATA2	[O]	TDM Encoder DATA2 Channel 3 & 4 (default)
	TDM ENC DAISY	[I]	TDM Encoder Daisy Chain Input
DATA4	TDM ENC DATA3	[O]	Optional TDM Encoder DATA3 Channel
DATA5	TDM ENC DATA4	[O]	Optional TDM Encoder DATA4 Channel

Table 16 - TDM Pin Connections

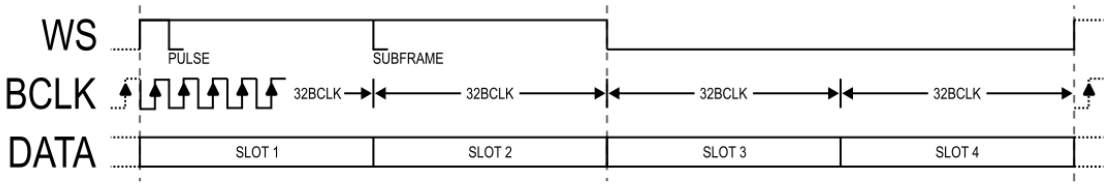


Figure 8 - TDM4 Mode

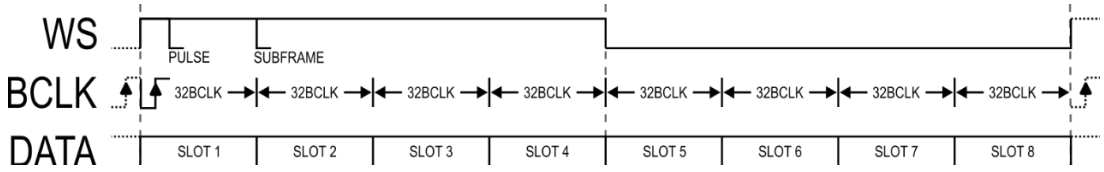


Figure 9 - TDM8 Mode

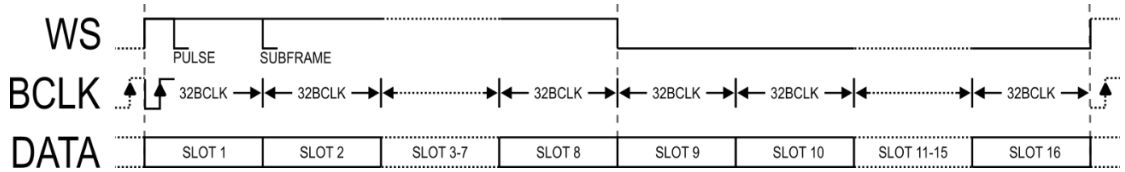


Figure 10 - TDM16 Mode

PDM Decoder (PDM Microphone Input)

The ES9841 can receive input audio from a PDM microphone using the integrated PDM decoder. To use the PDM microphone signal in software mode, ENABLE_PDM_MIC_DECODE must be set. PDM Microphone input is also supported in hardware mode, see GPIO Functions in Hardware Mode for more information.

Note: PDM_CLK_DIV will follow AUTO_FS_DETECT if enabled, and if AUTO_FS_DETECT is disabled, should be set to 7'd3 (default) for a 22.5792/24.576MHz MCLK and 7'd7 for a 45.1584/49.152MHz MCLK to ensure the PDM clock output is 3.072MHz (typical PDM Microphone frequency).

PDM Decoder (Microphone Input) Registers:

- Register 3[0] ENABLE_PDM_MIC_DECODE
- Register 21[4] PDM_MIC_INPUT_DATA_PHASE
- Register 21[5] PDM_MIC_INPUT_SAMPLE_EDGE
- Register 21[6] PDM_MIC_INPUT_SEL_CH12
- Register 21[7] PDM_MIC_INPUT_SEL_CH34
- Register 22[6:0] PDM_CLK_DIV

PDM Format

In PDM mode, there is a single PDM clock line and multiple PDM data lines containing two channels of data each. The channels can be swapped by setting Reg 21[4] PCM_MIC_INPUT_DATA_PHASE = 1'b1.

Pin Name	Function	Description
GPIO9	PDM MIC CLK	PDM Microphone Clock
DATA4	PDM MIC DATA 1	PDM Microphone Input DATA Channels 1 & 2
DATA5	PDM MIC DATA 2	PDM Microphone Input DATA Channels 3 & 4

Table 17 - PDM Decoder (Microphone Input) Pin Connections

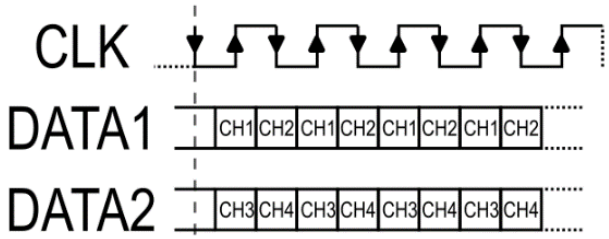


Figure 11 - PDM 4 Channel Format

S/PDIF Encoder

The ES9841 features a stereo auxiliary S/PDIF Encoder that can directly output a pair of channels (1/2, 3/4) which can be selected with SPDIF_CH_PAIR_SEL. The S/PDIF encoder can be enabled with ENABLE_SPDIF_ENCODE and output can be sent over any GPIO pin, see GPIO Configuration for more information.

The S/PDIF Encoder is auxiliary from the PCM/TDM Encoder, with the ability to be enabled with ENABLE_SPDIF_ENCODE while the PCM/TDM Encoder is running. To do this, ensure OUTPUT_SEL is still set to PCM or TDM, and set up the respective GPIO as the S/PDIF Encoders output.

The S/PDIF Encoder includes the ability to customize the 40-bits (5 bytes) of channel status bits one byte at a time by setting SPDIF_CS_BYTE_ADDR and SPDIF_CS_BYTE_DATA then toggling SPDIF_CS_WE to latch the single byte in the status bits.

S/PDIF Encoder Registers:

- Register 2[4] ENABLE_SPDIF_ENCODE
- Register 3[6:4] OUTPUT_SEL = 3'd5
- Register 23[1] SPDIF_CH_PAIR_SEL
- Register 24[7] SPDIF_CS_WE
- Register 24[2:0] SPDIF_CS_BYTE_ADDR
- Register 25 SPDIF_CS_BYTE_DATA

SPI Master Interface

The ES9841 features an SPI master interface that can be used as a generic I²C to SPI Transcoder. This allows the SPI Master to interface with a wide array of devices like flash memories, shift registers, and other SPI slave programmable ESS devices. The SPI master interface makes use of the GPIOs in the following table.

GPIO #	SPI Master Function
GPIO7	MISO Master (MISOM)
GPIO8	SS Master (SSM) or Chip Select Master (CSM)
GPIO10	SCLK Master (SCLKM)
GPIO11	MOSI Master (MOSIM)

Table 18 - SPI Master Interface GPIO Connections

There are three registers related to using the SPI master interface.

- Register 122 SPI_MASTER_CONFIG is used to start and end SPI transmissions and set the SPI master clock.
  - [7:4] SPI_M_PULSE_WIDTH – sets the SPI clock frequency
  - [3] SPI_M_EN – Enables the SPI Master interface
  - [2] SPI_M_MODE – Switches the SPI master between Mode 0 (default) and Mode 3
  - [1] SPI_M_SEND_BYTE – Used to manually send/receive SPI bytes.
  - [0] SPI_M_START – Starts and SPI transaction, pulls SSM (GPIO8) low
- Register 123 SPI_MASTER_DATA_OUT contains the data byte to be sent from the SPI master interface.
- Register 247 SPI_MASTER_DATA_IN contains the data byte received by the SPI master interface.

When the chip is powered on or reset the chip select output (GPIO8) will be set low by default. When Register 122 [3] SPI_M_EN is set high, enabling the SPI master interface, the chip select will output high.

SPI Write

Writing data on the SPI bus requires 2+n write-register commands where n is the number of bytes to be sent in one SPI transaction. To efficiently write multiple bytes of data sequentially, Register 122 [1] SPI_M_SEND_BYTE must remain low for automatic SPI data output. Each time Register 123 SPI_M_DATA_OUT is written during an SPI transaction the data will automatically be sent out of the SPI master interface at the end of the write-register command.

A single byte SPI transmission would be sequenced as follows:

1. Setup Register 122 SPI MASTER CONFIG
   - [7:4] SPI_M_PULSE_WIDTH sets the SPI clock speed
   - [3] SPI_M_EN = 1'b1 enables the SPI master
   - [2] SPI_M_MODE selects between SPI modes 0 and 3
   - [1] SPI_M_SEND_BYTE = 1'b0 for automatic operation
   - [0] SPI_M_START prepares the SPI master interface to initiate an SPI transmission.
2. Write a byte of data to Register 123. This will automatically start the SPI transaction.
   - After receiving the write-register command the chip select output (GPIO8) is set low after 2 MCLK cycles.
   - The SPI clock will begin half an SPI clock cycle plus one MCLK cycle after the chip select is set low.
   - The SPI master interface will output the 8 bits of data and afterwards the SPI clock will remain idle, and the chip select low.
3. Resetting Register 122 [0] SPI_M_START low will end the SPI transaction by setting the chip select high.

To write multiple bytes of data in one SPI transaction repeat step 2 for each byte. As an example, the following sequence will write two sequential bytes to an SPI device like a Serial-In to Parallel-Out (SIPO) Shift Register.

```
void I²C_WriteByte(uint32_t data1, uint16_t data2)
{
  I²C_WriteReg(122, 0x19);  // Start SPI
  I²C_WriteReg(123, data1);  // Output data1
  I²C_WriteReg(123, data2);  // Output data2

  I²C_WriteReg(122, 0x18);  // End SPI
}
```

SPI Read

The data byte received on the SPI master interface is stored in Register 247 SPI_MASTER_DATA_IN. The last byte of data stored can be read back at any time with a read-register command.

Sequential SPI reads can be efficiently performed by automatically triggering after each read-register command while the Register 122 [1] SPI_M_SEND_BYTE bit remains low. In this configuration when Register 247 is readback the data currently in it will be transmitted on the I²C or SPI slave interfaces and immediately after the read-register command finishes the SPI master interface will automatically trigger another sequence of 8 bits to load in the next byte of data.

During a read-register command whatever data is already stored in Register 123 SPI_MASTER_DATA_OUT will be output again for each read-register command on Register 247.

The following example sequence reads two sequential 8-bit values from a Parallel-In to Serial-Out (PISO) Shift Register.

```
uint16_t I²C_ReadBytes()
{
  I²C_WriteReg(122, 0x19);               // Start SPI

  I²C_WriteReg(123, 0x00);               // Dummy data to load in first byte from Shift Register
  uint8_t in1 = I²C_ReadReg(247);        // Reads first byte from ES9841 and then loads second byte from Shift Register
  I²C_WriteReg(122, 0x18);               // End SPI
  uint8_t in2 = I²C_ReadReg(247);        // Reads second byte from ES9841

  return (in1 << 8 | in2);               // Return 16-bit data
}
```

SPI Simultaneous Read and Write

In the default automatic mode, it is not possible to write new data while the data is being read back on the I²C or SPI slave interfaces. However, there is way to sequence the commands to be able to both read and write data at the same time without the automatic sequencing:

1. While the SPI master is not currently active, load the first byte of data into Register 123
2. Enable the SPI output with Register 122 and set bit [1] high to begin the SPI transaction and output the first byte of data
3. While Register 122 [1] remains high, the first data byte received can be readback (Register 247) without automatically triggering another byte sequence
4. The second byte of data to be transmitted can then be loaded into Register 123, again without automatically triggering a byte sequence.
5. Then Register 122 [1] must be set low and back high again to trigger the next SPI sequence. The sequence will immediately follow the write-register command setting that bit high.
6. Afterwards the data received can be readback from Register 247 and the next byte loaded into Register 123 again.
7. To end the SPI transaction set Register 122 [0] low and the chip select will immediately be set high.

As long as Register 122 [1] is high, data can be written and read from the SPI master interface without automatically trigger the SPI master output. Any time the bit is set high the SPI master interface will output the data currently in Register 123 and replace the data in readback Register 247. This process to manually read and write takes four read/write register commands for each byte of data to be transmitted on the SPI master interface.

```
I²C_WriteReg(123, 0x03);      // Load first data byte
I²C_WriteReg(122, 0x1B);      // Start SPI
I²C_ReadReg(247);             // Read first data byte

I²C_WriteReg(123, 0x12);      // Load second data byte
I²C_WriteReg(122, 0x19);      // Toggle Send Byte bit
I²C_WriteReg(122, 0x1B);
I²C_ReadReg(247);             // Read second data byte

I²C_WriteReg(122, 0x18);      // End SPI
```

SPI Shift Register Control

The ES9841s SPI Master Interface can interact with a multitude of SPI Devices like a Shift Registers effectively adding a serial to parallel converter to the ES9841. This can be useful for extending the amount of GPIO's

For more information on the SPI Master Interface and its application please ask your FAE or Distributor for the Application Note.

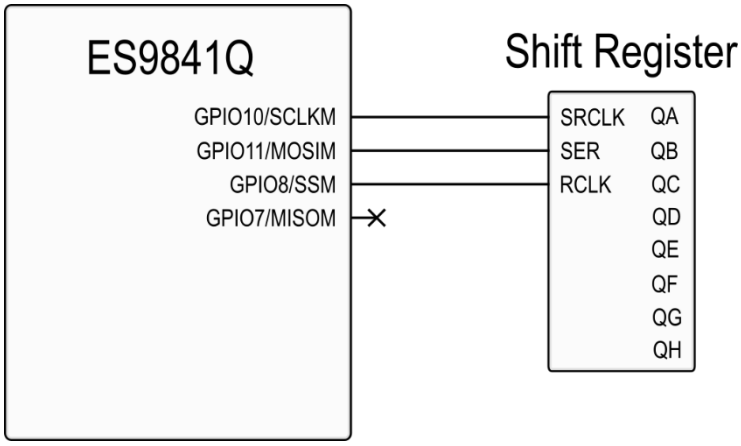


Figure 12 - Example SPI Shift Register Schematic

Digital Signal Path

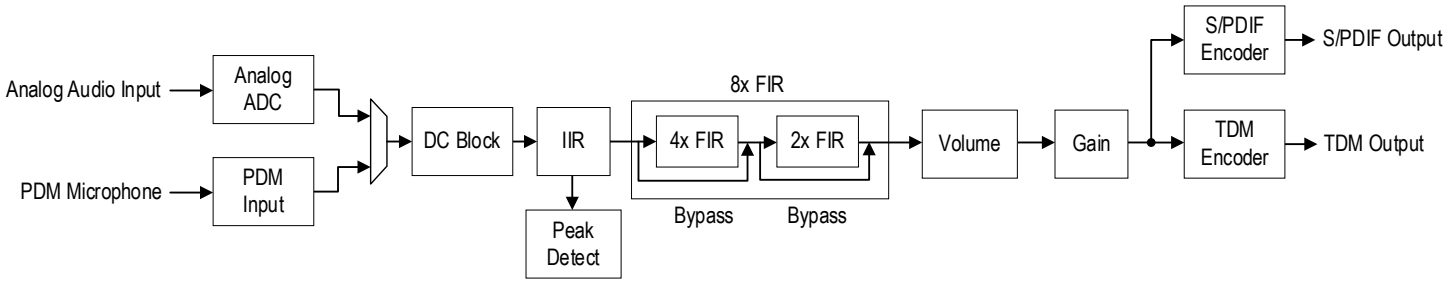


Figure 13 - Digital Signal Path

DC Block

The integrated DC Blocking filter exhibits a high cutoff frequency (-3dB @ 0.25Hz).

DC Blocking Registers

- Register 76[4] DC_BLOCK_EN_CH1
- Register 76[5] DC_BLOCK_EN_CH2
- Register 76[6] DC_BLOCK_EN_CH3
- Register 76[7] DC_BLOCK_EN_CH4

Peak Detect

If the peak level of the ES9841 input rises above the programmed PEAK_THRESH_CHx value, the corresponding peak flag will be set. The level will decay at a rate based off the value of PEAK_DECAY_RATE. The peak detection can be toggled on or off using the PEAK_DETECT_EN_CHx registers. The peak can be read from the PEAK CHx READ registers and a flag will be set on the PEAK_FLAG_CHx registers. Normal flag registers will unset the flag once it is no longer asserted except the PEAK_FLAG_LAT_CHx registers which will stay set until it is cleared with CLEAR_PEAK_DET_CHx.

GPIO pins can be configured to output the state of any latched peak flags if MASK_PEAK_DET_CHx is set for the corresponding channel.

Peak Enable Registers

- Register 98[3:0] PEAK_DETECT_EN_CHx

Peak Decay Rate and Threshold Registers

- Register 99[4:0] PEAK_DECAY_RATE
- Register 100-103[7:0] PEAK_THRESH_CH1
- Register 100-103[15:8] PEAK_THRESH_CH2
- Register 100-103[23:16] PEAK_THRESH_CH3
- Register 100-103[31:24] PEAK_THRESH_CH4

Peak Flag GPIO Registers

- Register 32[3:0] MASK_PEAK_DET_CHx

Peak Flag and Read Registers

- Register 236-237 PEAK_LEVEL_CH1
- Register 238-239 PEAK_LEVEL_CH2
- Register 240-241 PEAK_LEVEL_CH3
- Register 242-243 PEAK_LEVEL_CH4
- Register 235[7:4] PEAK_FLAG_CHx
- Register 235[3:0] PEAK_FLAG_LAT_CHx
- Register 33[3:0] CLEAR_PEAK_DET_CHx

$$N(t) = N_0 exp\left(\frac{-MCLK\_24M * t}{2^{decay\_rate+9}}\right)$$

$$N(t) = N_0 - \frac{20 * MCLK\_24M * t}{ln(10) * 2^{decay\_rate+9}}[dB]$$

$$\frac{dN}{dt} = -\frac{N * MCLK\_24M}{2^{decay\_rate+9}}[1/s]$$

$$\text{threshold [dB]} = 20 \cdot \log10\left(\left(\frac{PEAK\_THRESH\_CHx}{2^8 - 1}\right) \cdot \left(\frac{32}{30}\right)\right)$$

N_0: Initial Level
N(t): Level at time t
decay_rate = Reg 99[4:0]PEAK_DECAY_RATE
MCLK_24M = 22.5792/24.576MHz
(Reg 5[4] MCLK_24M_DIV2 must be set if using a 45.1584/49.152MHz MCLK)

Volume Control

The Volume Control is intended for use during audio playback. Each channel can be digitally attenuated from +0dB to -127dB in 0.5dB steps. When a new volume level is set, the attenuation circuit will ramp softly to the new level at a rate specified in the VOLUME UP RAMP RATE and VOLUME DOWN RAMP RATE registers. To mute a channel, set the respective VOLUME CHx to 8'hFF.

The ES9841 also features the ability to invert the volume control phase as well as control all channel volumes with the CH1 volume control.

Volume Control Registers

- Register 81-84 VOLUME_CHx
- Register 88 VOLUME_UP_RAMP_RATE
- Register 89 VOLUME_DOWN_RAMP_RATE
- Register 87[3:0] VOL_PHASE_INV_CHx
- Register 86-85[15] MONO_VOLUME

Gain Control

The ES9841 has a digital pre-gain of up to +42dB in 6 dB (+6,+12,+18,+24,+30,+36,+42) steps.

Gain Registers

- Register 86-85 DIGITAL GAIN

The digital pre-gain and volume control can be used together for finer resolution. The below figure shows the available ranges:

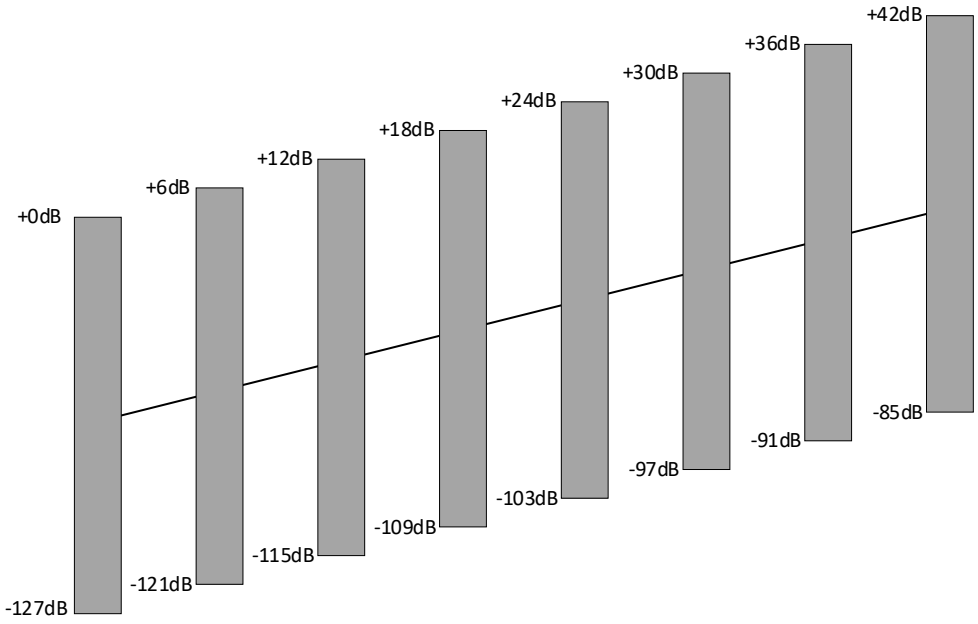


Figure 14 - ES9841 Volume and Gain Range

8x FIR Filter

Selection of the 8x interpolation filter is chosen from 8 pre-programmed filters. The 2x and 4x filter can be bypassed individually or together. For more information on filters see the Pre-Programmed Digital Filters section.

8x FIR Registers

- Register 74[7:5] FILTER_SHAPE
- Register 74[4] BYPASS_FIR2X
- Register 74[3] BYPASS_FIR4X

IIR Filter

The IIR filter can be bypassed using Register 74[2:0] BYPASS_IIR

GPIO Configuration

GPIO_CONFIG	Function	I/O Direction
0	Analog Outputs Off	Shutdown
1	Output 1'b0	Output
2	OR of Status Bits	Output
3	Clock Valid	Output
4	S/PDIF Stream	Output
5	PWM1	Output
6	PWM2	Output
7	PWM3	Output
8	Reserved	NA
9	Reserved	NA
10	Mute ADCs	Input
11	BCK WS Fail Flag	Output
12	CH1 Detection Flag	Output
13	CH2 Detection Flag	Output
14	CH3 Detection Flag	Output
15	CH4 Detection Flag	Output

Table 19 - GPIO Configuration

Analog Outputs Off

The GPIO is shutdown and has no functionality.

Output 1'b0

Outputs a constant 1'b0.

To output a constant 1'b1, set the respective GPIOx_INV (Reg 57-58) to invert the signal.

OR of Status Bits

Outputs a bitwise OR of all masked status bits.

Relevant Registers:

- Register 32[7:4] MASK_ADC_OVERLOAD_CHx
- Register 32[3:0] MASK_PEAK_DET_CHx
- Register 33[7:4] CLEAR_ADC_OVERLOAD_CHx
- Register 33[3:0] CLEAR_PEAK_DET_CHx

Clock Valid

Outputs HIGH if a valid MCLK source is detected. Outputs LOW when clock is removed or not present.

Relevant Registers:

- Register 7[0] CLK_FAULT_DET_EN must be asserted for the clock valid flag to operate.

S/PDIF Stream

Outputs the S/PDIF stream from the S/PDIF encoder.

PWM Signal

Outputs a configurable PWM signal. The frequency and duty cycle of the PWM signal can be calculated with the following equations:

$$frequency\ [Hz] = \frac{MCLK}{PWMx\_FREQ + 1}$$

$$Duty\ Cycle\ [\%] = \left(\frac{PWMx\_COUNT}{PWMx\_FREQ + 1}\right) \times 100$$

Relevant Registers:

- Registers 64, 67, 70 PWMx_COUNT
- Register 65-66, 68-69, 71-72 PWMx_FREQUENCY

CHx Detection Flags

Outputs a detection flag for a specific channel, either the Peak Detector or ADC Overload flags can be output. The live or latched version of the flags can be output. By default, the latched peak detect flag is output.

Relevant Registers:

- Register 63[7:4] LIVE_DETECT_CHx
- Register 63[3:0] DETECT_FLAG_SEL_CHx

Pre-Programmed Digital Filters

The ES9841 has 8 pre-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates. (See Register 74[7:5] FIR_FILTER_SHAPE for configuration)

#	Filter	Description
1	Minimum Phase (default)	Version 2 of minimum phase fast roll-off (#6) with less ripple and more image rejection
2	Linear Phase Apodizing Fast Roll-Off	Full image rejection by FS/2 to avoid any aliasing, with smooth roll-off starting before 20k.
3	Linear Phase Fast Roll-Off	Sabre legacy filter, optimized for image rejection @ 0.55FS
4	Linear Phase Fast Roll-Off Low-Ripple	Sabre legacy filter, optimized for in-band ripple
5	Linear Phase Slow Roll-Off	Sabre legacy filter, optimized for lower latency, but symmetric impulse response
6	Minimum Phase Fast Roll-Off	Low latency, minimal pre ringing and low passband ripple, image rejection @ 0.55FS
7	Minimum Phase Slow Roll-Off	Lowest latency at the cost of image rejection
8	Minimum Phase Slow Roll-Off Low Dispersion	Provides a nice balance of the low latency of minimum phase filters and the low dispersion of linear phase filters. Minimal pre-ringing is added to achieve the low dispersion in the audio band.

Table 20 - Pre-Programmed Digital Filter Descriptions

Note: Minimum phase filters are asymmetric filters that work to minimize the pre-echo of the filter, while still maintaining an excellent frequency response and they peak earlier than linear phase filters, resulting in a lower group delay. Minimum phase filters usually feature zero cycles of pre-echo, which can result in improved audio quality.

PCM Filter Latency

The following table shows the simulated latency of each filter at multiple sampling rates. The filter latency is measured from the time an external impulse is presented on the ADC input pins (IN_Px/IN_Nx) to the start of the corresponding WS frame on the DATA1 pin.

Filter Shape \ Frequency [kHz]	44.1 / 48	88.2 / 96	176.4 / 192	352.8 / 384
Minimum Phase (default)	4.37 / FS	4.50 / FS	4.74 / FS	5.36 / FS
Linear Phase Apodizing Fast Roll-Off	34.25 / FS	34.38 / FS	34.62 / FS	35.24 / FS
Linear Phase Fast Roll-Off	34.38 / FS	34.50 / FS	34.75 / FS	35.36 / FS
Linear Phase Fast Roll-Off Low-Ripple	34.00 / FS	34.13 / FS	34.37 / FS	34.99 / FS
Linear Phase Slow Roll-Off	7.00 / FS	7.12 / FS	7.37 / FS	7.98 / FS
Minimum Phase Fast Roll-Off	4.50 / FS	4.62 / FS	4.87 / FS	5.48 / FS
Minimum Phase Slow Roll-Off	3.37 / FS	3.50 / FS	3.74 / FS	4.36 / FS
Minimum Phase Slow Roll-Off Low Dispersion	5.25 / FS	5.37 / FS	5.62 / FS	6.23 / FS

Table 21 - PCM Filter Latency

PCM Filter Properties

Minimum Phase					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.45 FS	Hz
Stop band	-101.2 dB	0.55 FS			Hz
Group Delay		2.90/FS		9.23/FS	s
Flatness (ripple)	0.0017				dB

Linear Phase Apodizing					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.41 FS	Hz
Stop band	-108.6 dB	0.50 FS			Hz
Group Delay			33.25/FS		s
Flatness (ripple)	0.0022				dB

Linear Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.45 FS	Hz
Stop band	-115.5 dB	0.55 FS			Hz
Group Delay			33.38/FS		s
Flatness (ripple)	0.0025				dB

Linear Phase Fast Roll-Off Low Ripple					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.45 FS	Hz
Stop band	-82.57 dB	0.55 FS			Hz
Group Delay			33.00/FS		s
Flatness (ripple)					dB

Linear Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.26 FS	Hz
Stop band	-85.15 dB	0.75 FS			Hz
Group Delay			6.05/FS		s
Flatness (ripple)					dB

Minimum Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.45 FS	Hz
Stop band	-101.3 dB	0.55 FS			Hz
Group Delay		2.95/FS		9.42/FS	s
Flatness (ripple)	0.0034				dB

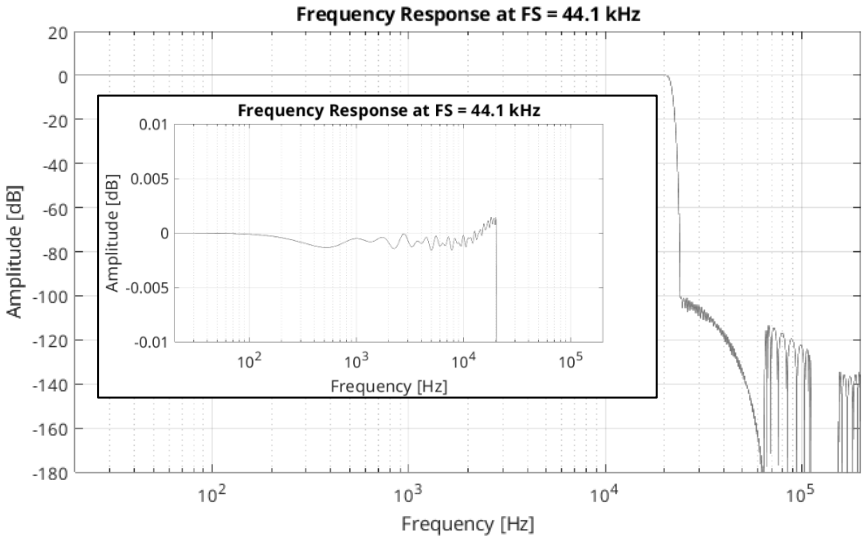
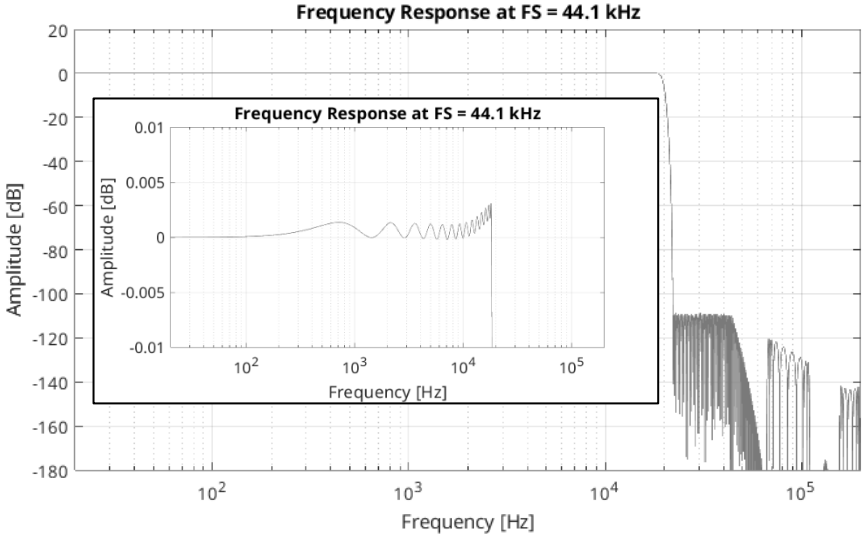
Minimum Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.28 FS	Hz
Stop band	-90.37 dB	0.82 FS			Hz
Group Delay		2.03/FS		3.51/FS	s
Flatness (ripple)					dB

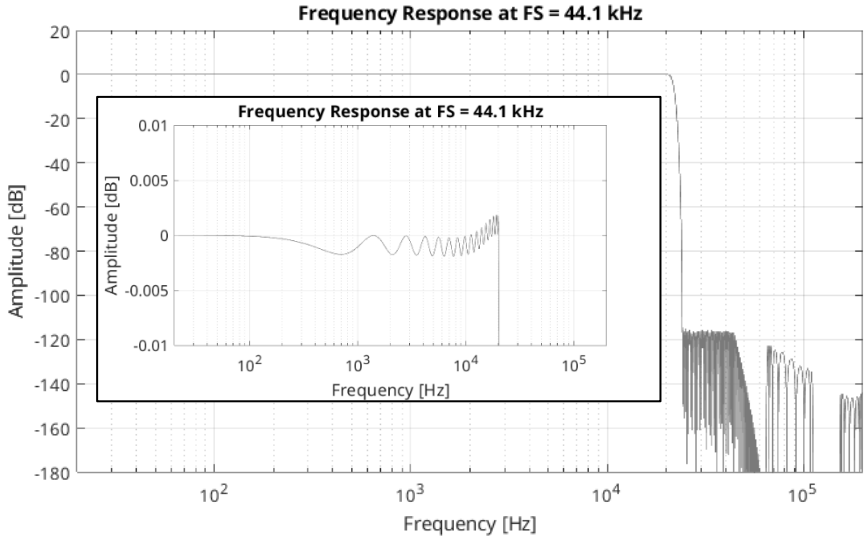
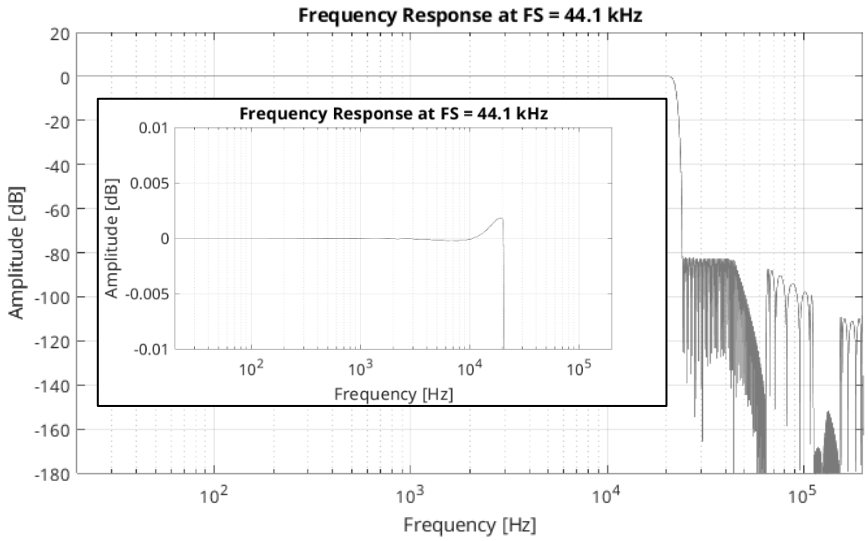
Minimum Phase Slow Roll-Off Low Dispersion					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.28 FS	Hz
Stop band	-98.6 dB	0.82 FS			Hz
Group Delay		4.12/FS		4.38/FS	s
Flatness (ripple)					dB

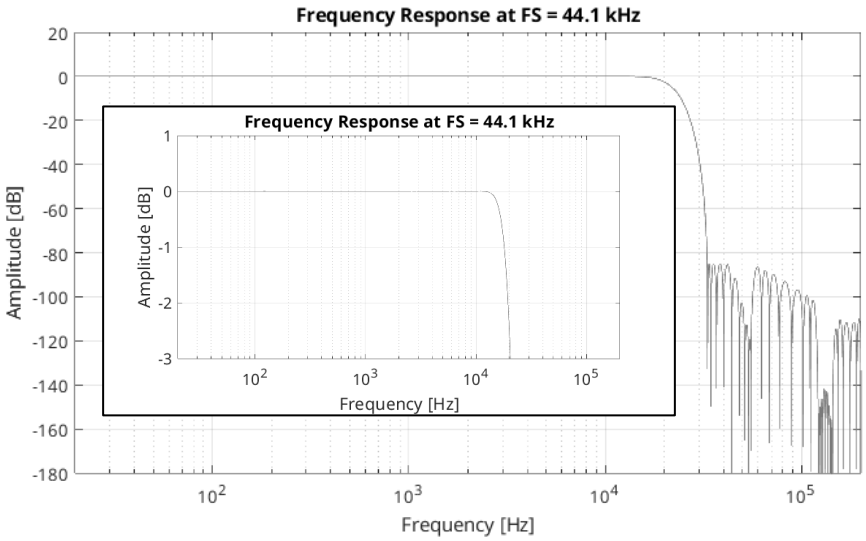
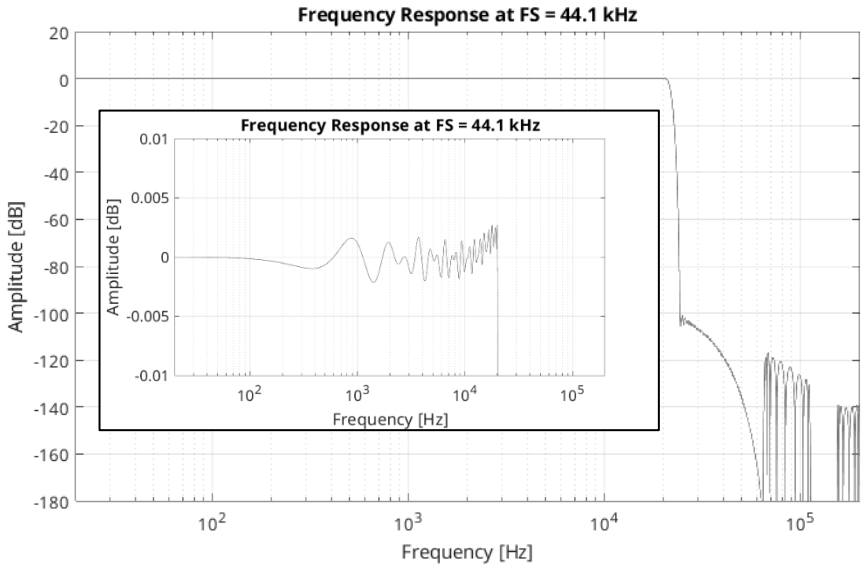
Table 22 - PCM Filter Properties

PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Frequency Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

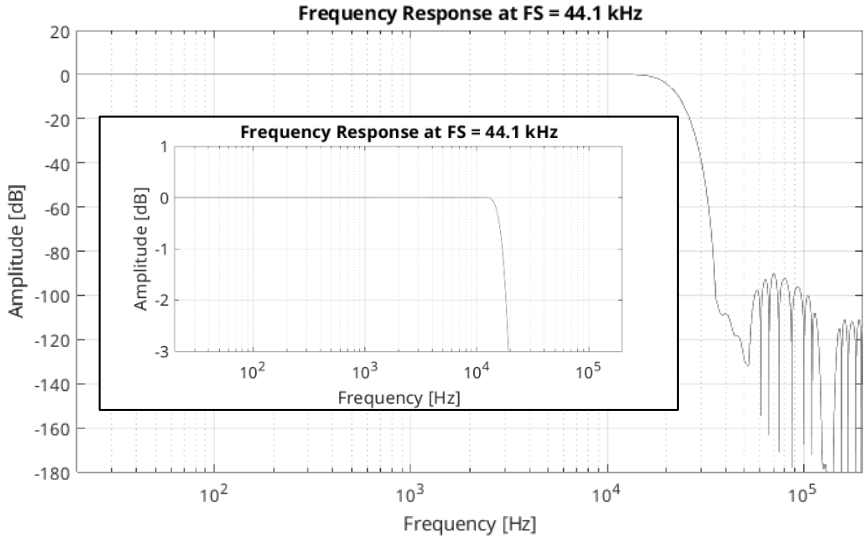
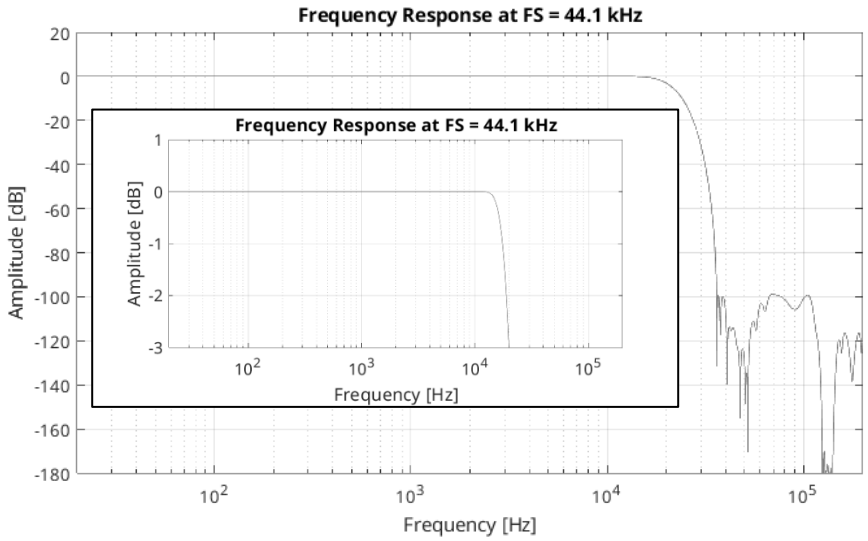
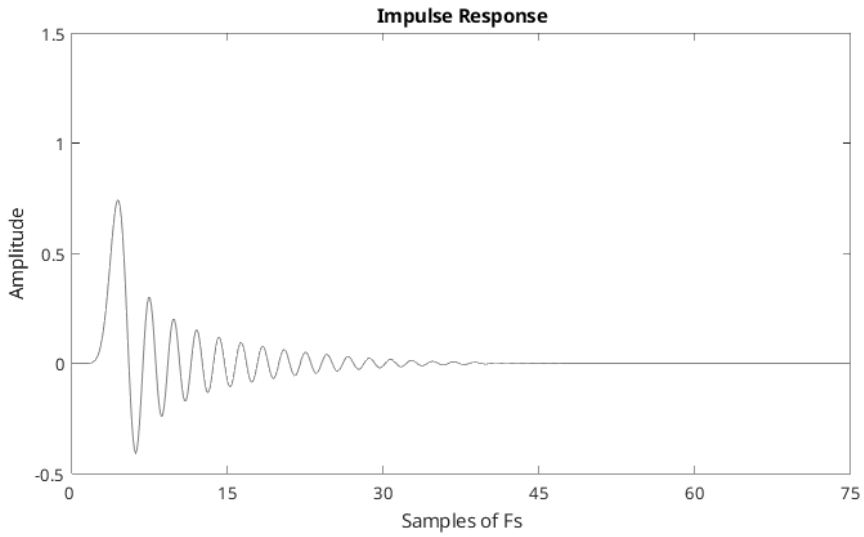
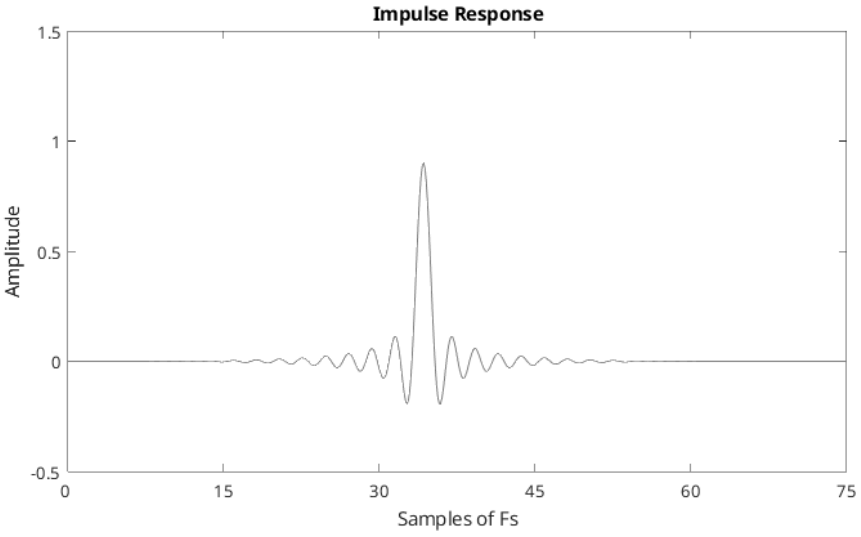
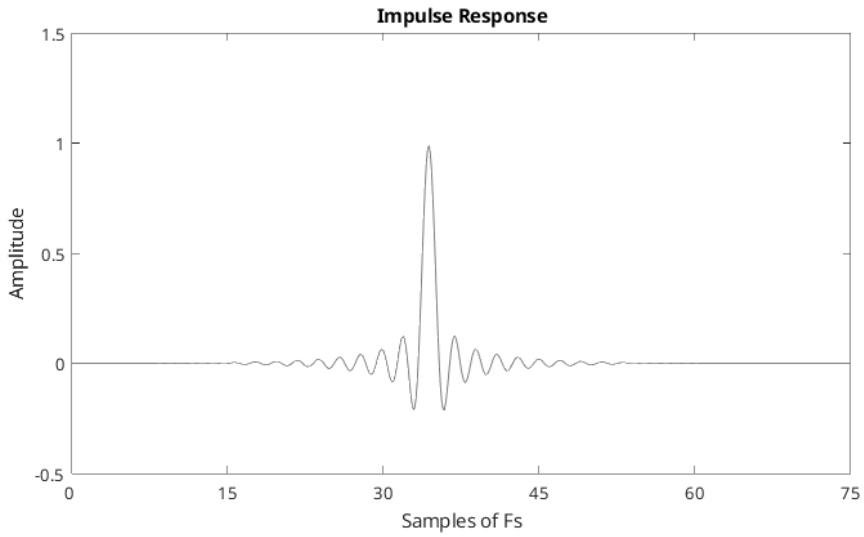
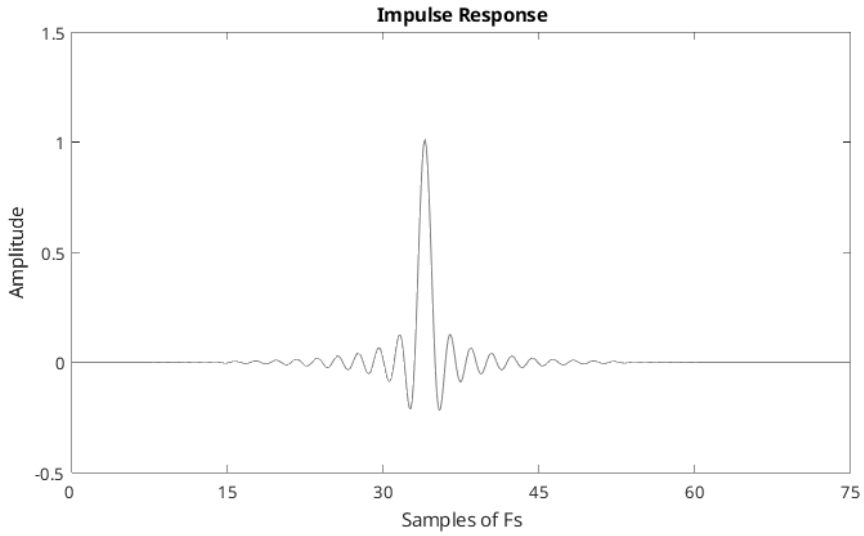
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

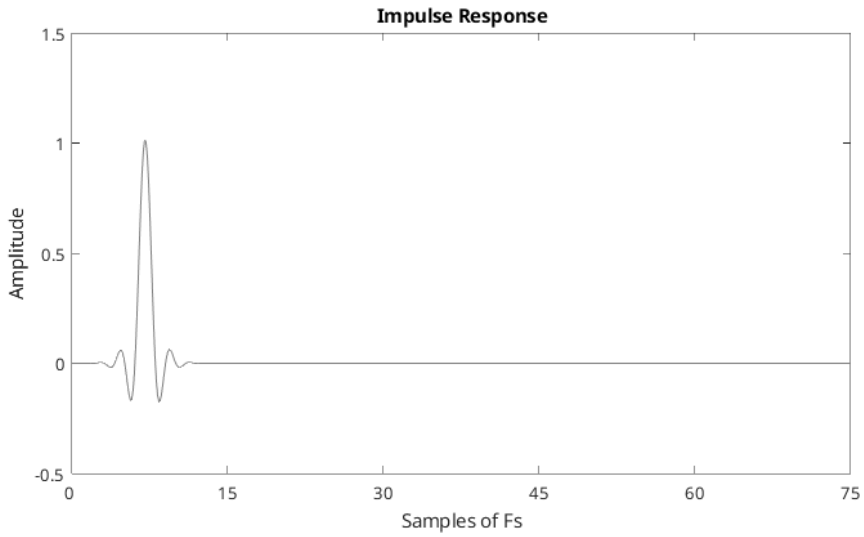
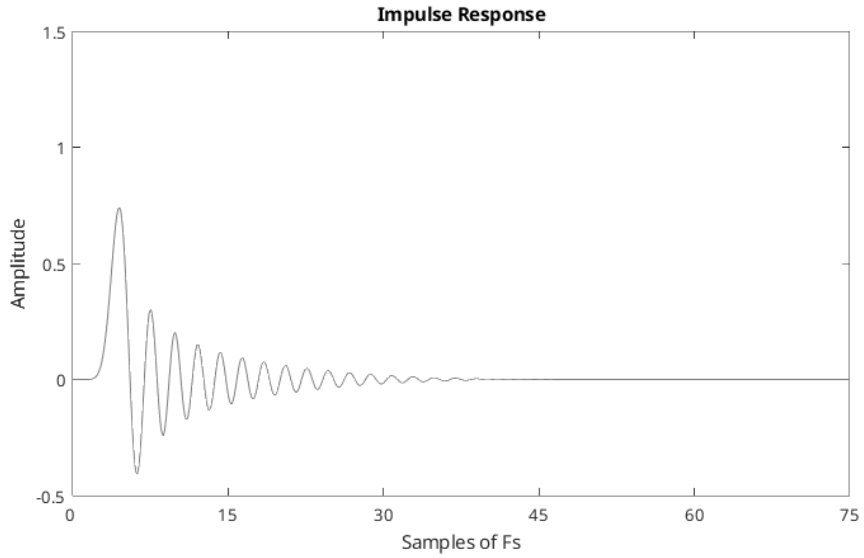
Table 23 - PCM Filter Frequency Response

PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. They show the decimation path prior to down-sampling to 1FS and are scaled accordingly. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

Filter	Impulse Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

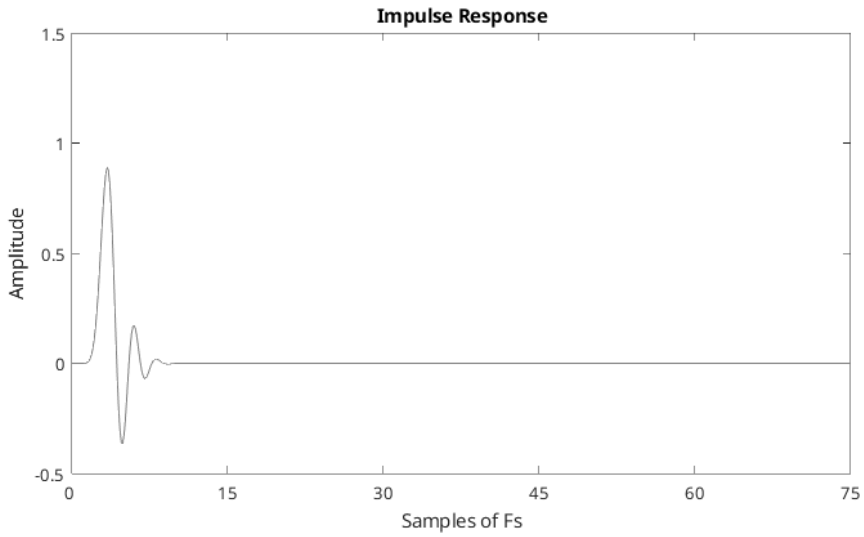
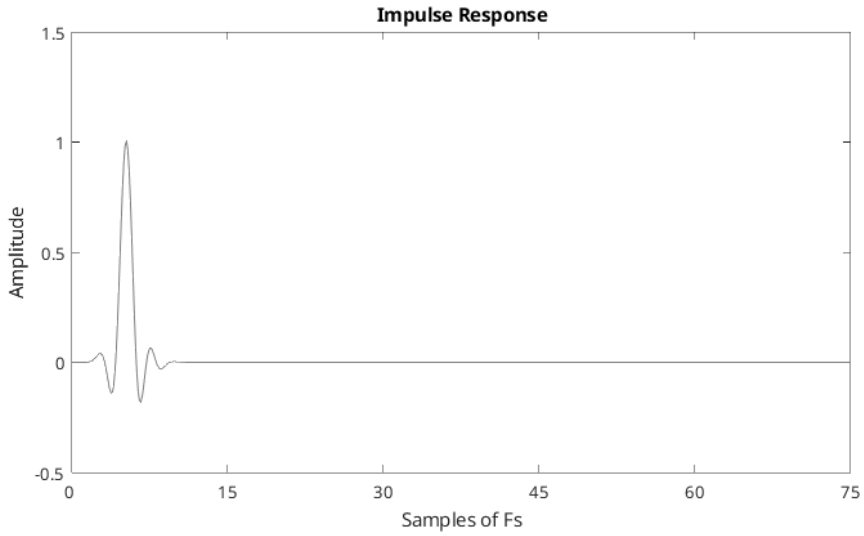
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

Table 24 - PCM Filter Impulse Response

64FS Mode

When the MCLK/FS ratio is required to be 64, it is necessary for the ES9841 to be in 64FS mode. 64FS Mode can be enabled by setting:

Software Register

- Register 1[2] ENABLE_64FS_MODE = 1'b1
  - Manually enables 64FS mode
  - Should be used with high sample rates like 705.6kHz & 768kHz
- Register 1[0] AUTO_FS_DETECT = 1'b1
  - Sets the MCLK_128FS divider according the MCLK/FS ratio
  - Automatically enables 64FS mode when MCLK/MCLK_128FS ratio is 64
- 64FS mode can be blocked when AUTO_FS_DETECT is enabled by setting:
  - Register 1[1] AUTO_FS_DETECT_BLOCK_64FS = 1'b1

Minimum Phase 64FS Mode Latency

The following table shows the simulated latency at 352.8/384 kHz and 705.6/768 kHz sample rate. Measurements were taken from the external impulse response prior to being down sampled to 1FS. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

Digital Filter \ Frequency [kHz]	352.8 / 384	705.6 / 768
Minimum Phase Double Rate	3.49 / FS	3.72 / FS

Table 25 - Minimum Phase 64FS Latency

Minimum Phase 64FS Properties

Minimum Phase 64FS Mode					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.44 FS	Hz
Stop band	-59.13 dB	0.68 FS			Hz
Group Delay		1.43/FS		3.45/FS	s
Flatness (ripple)					dB

Table 26 - Minimum Phase 64FS Properties

Minimum Phase 64FS Frequency Response

This filter gets selected automatically when MCLK/FS = 64. The following frequency response was obtained from software simulations with a sample rate of 705.6kHz

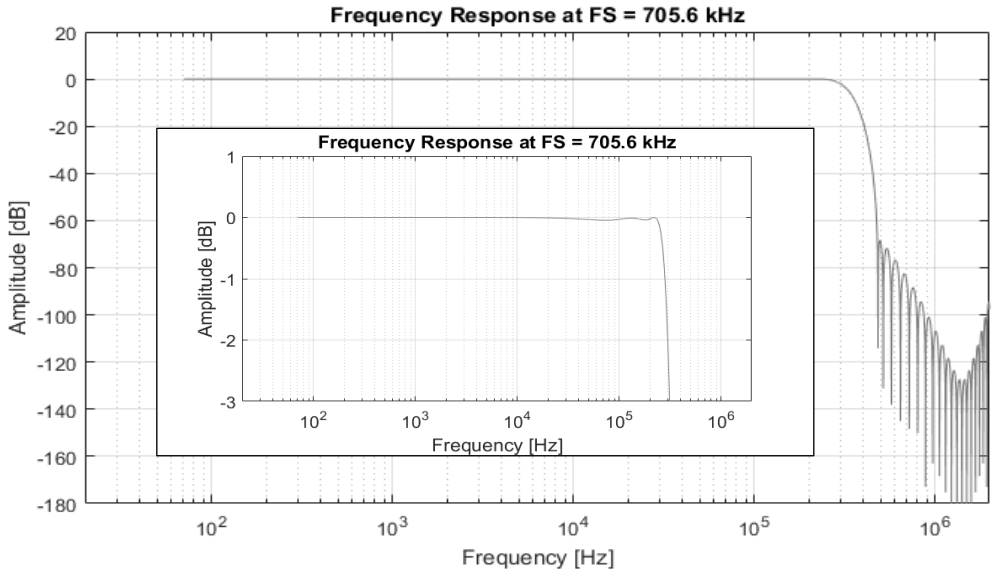


Figure 15 - Minimum Phase 64FS Frequency Response

Minimum Phase 64FS Impulse Response

The following impulse responses were obtained from software simulations of these filters. They show the decimation path prior to down-sampling to 1FS and are scaled accordingly. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

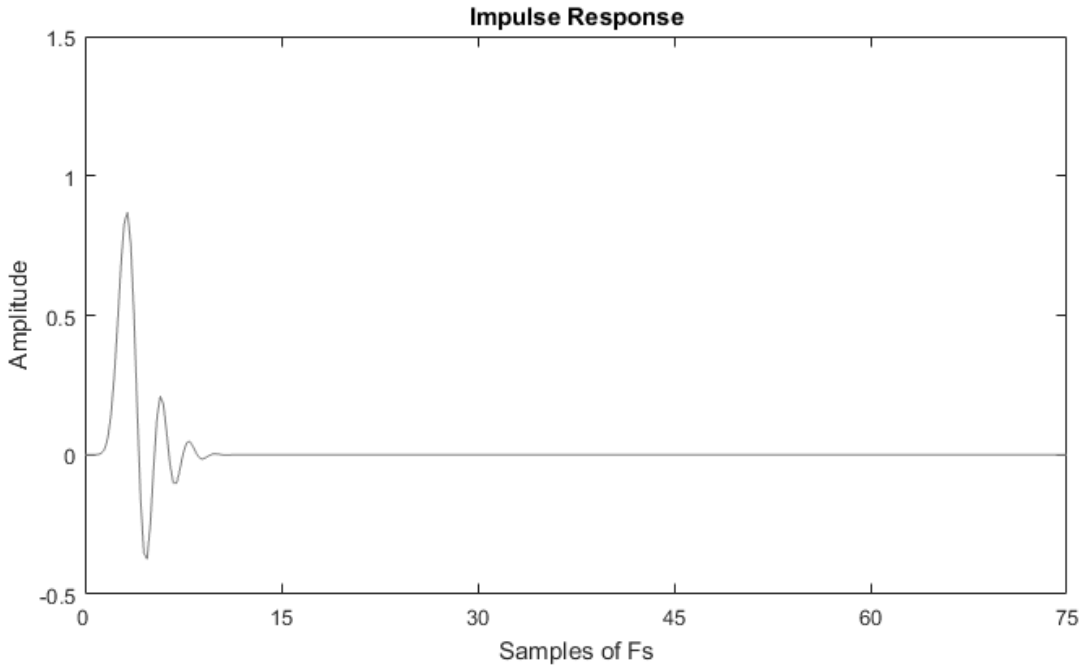


Figure 16 - Minimum Phase 64FS Impulse Response

TDM Encoder Daisy Chain

The ES9841s TDM Encoder supports connecting multiple devices together in a daisy chain configuration. This allows the digital output from one chip to be input to the next, with the last chip on the chain outputting the final data on the serial line.

To enable Daisy Chain, set Register 15[7] TDM_ENC_DAISY_CHAIN to 1. This will configure DATA2 as the output and DATA3 as the input. The output pin can be changed to DATA5 by setting TDM_DAISYLINE_SEL = 1'b1. The figure below shows how several ES9841s can be combined in daisy chain mode.

Note: Each TDM Encoder Line must be configured using Register 11-14 to output on the respective pin chosen by TDM_DAISYLINE_SEL (DATA2 or DATA5).

Note: The input to the first ES9841 (DATA3) must be grounded.

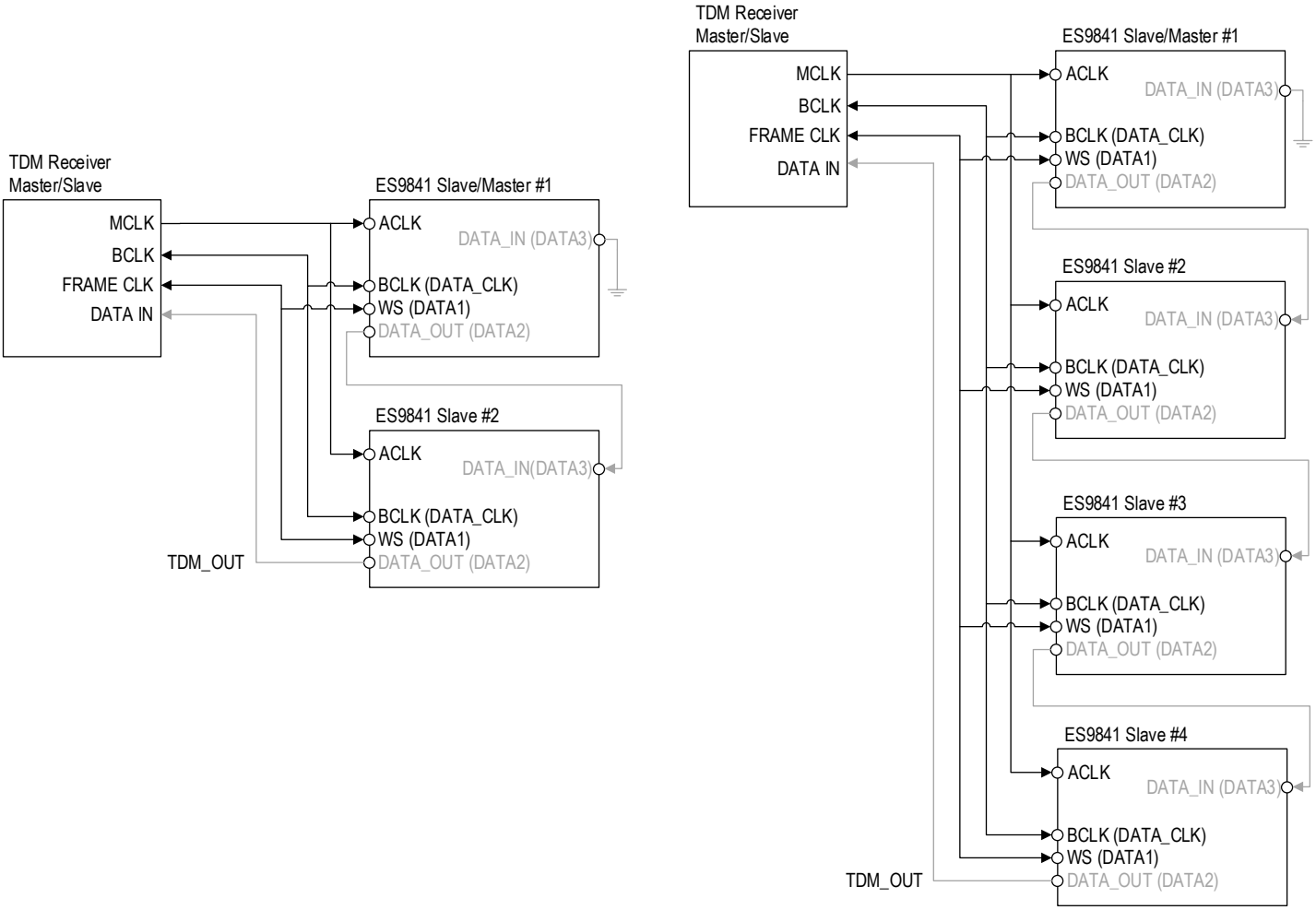
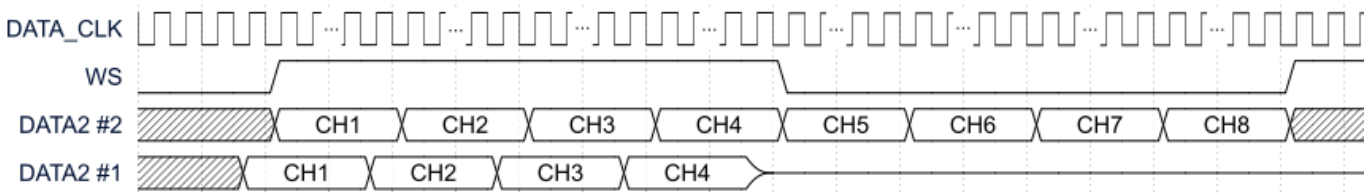


Figure 17 - Example Connection for TDM Encoder Daisy Chain Mode

TDM Encoder Daisy Chain Registers:

- Register 9[4:0] TDM_CH_NUM
- Register 15[7] TDM_ENC_DAISY_CHAIN
- Register 15[5] TDM_DAISYLINE_SEL
- Register 15[4:0] TDM_ENC_DATA_LATCH_ADJ

Using Daisy Chain incurs a single bit-clock delay as data passes each device in the chain. To maintain a coherent TDM frame at the final output, an inverse timing offset must be applied to each device through Register 15[4:0] TDM_ENC_DATA_LATCH_ADJ.



Clock Distribution

The ES9841 includes features for selection and manipulating the input clock source.

The minimum MCLK frequency is 22.579MHz.

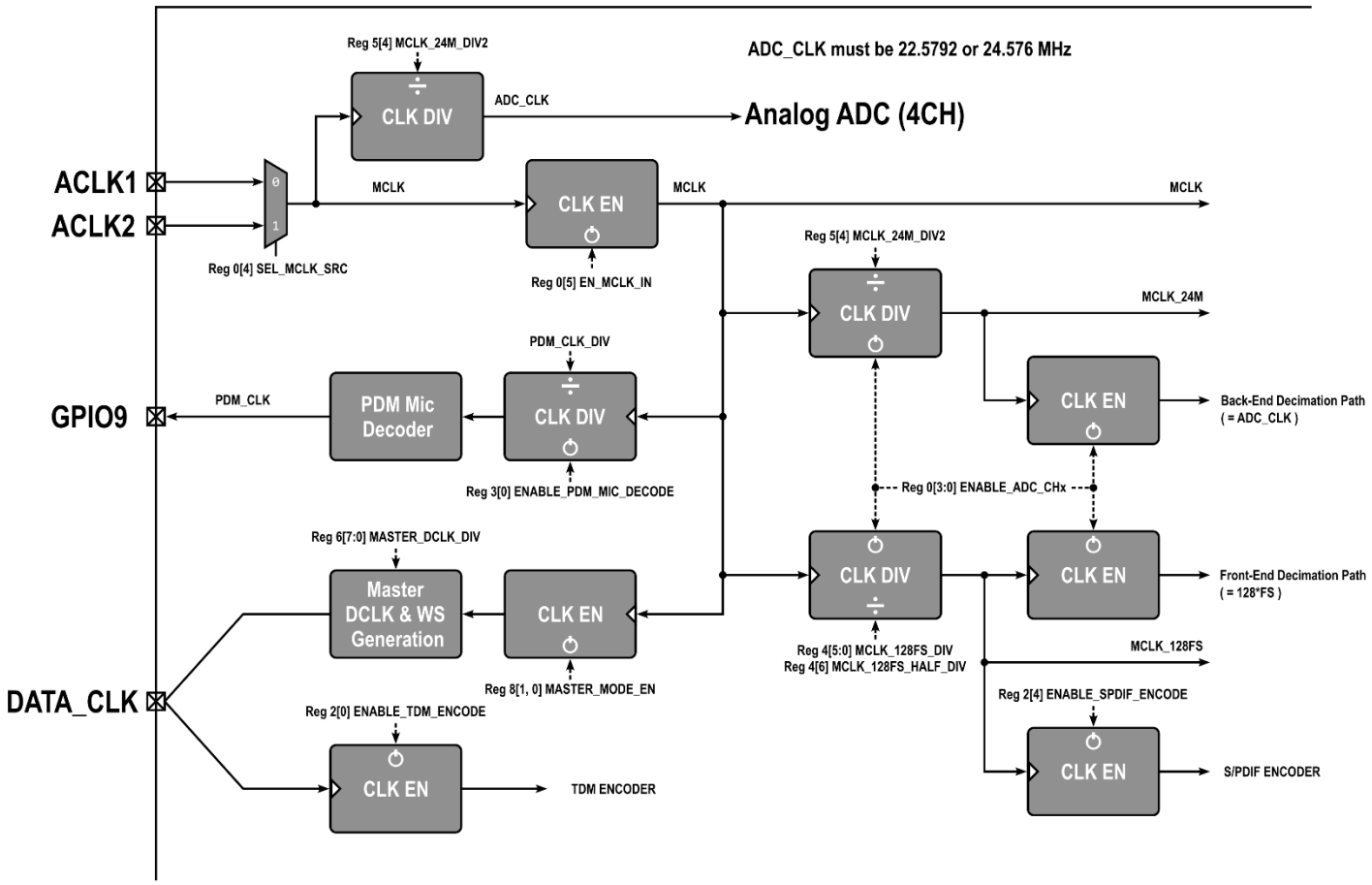


Figure 18 - Clock Distribution

The following list shows the various clocks of the ES9841 and the associated registers for configuration.

ADC_CLK

ADC_CLK must be maintained to be between 22.5893MHz & 24.576MHz

- Register 5[4] MCLK_24M_DIV2

MCLK

- Register 0[4] SEL_MCLK_SRC

MCLK_24M (Back-End Decimation Path)

MCLK_24M is equal to ADC_CLK.

- Register 5[4] MCLK_24M_DIV2
- Register 0[3:0] ENABLE_ADC_CHx

MCLK_128FS (Front-End Decimation Path)

- Register 4[5:0] MCLK_128FS_DIV
- Register 4[6] MCLK_128FS_HALF_DIV
- Register 0[3:0] ENABLE_ADC_CHx

Master DCLK & WS Generation

- Register 8[0] PCM_MASTER_MODE_EN
- Register 6[7:0] MASTER_DCLK_DIV

TDM Encoder

- Register 2[0] ENABLE_TDM_ENCODE

PDM Decoder (Microphone Input)

- Register 3[0] ENABLE_PDM_MIC_DECODE

SPDIF Encoder

- Register 2[4] ENABLE_SPDIF_ENCODE

THD Compensation

The ES9841 has integrated THD compensation to add or correct second and third harmonics that may be present on the output signal. The compensation is controlled by two 16-bit coefficients, one for first order and one for second order harmonics, located in Registers 90-97.

The following equation displays how the second and third harmonics are affected by the C2 and C3 values:

$$output = x + c2 * x^2 + c3 * x^3$$

THD Compensation Coefficient Registers

- Registers 90-91: THD COMP C2 CH1/2
- Registers 92-93: THD COMP C3 CH1/2
  - This register's value is internally XORed with 0xFFD8
- Registers 94-95: THD COMP C2 CH3/4
- Registers 96-97: THD COMP C3 CH3/4
  - This register's value is internally XORed with 0xFFD8

Analog Features

APLL

The ES9841 has a built in Analog PLL (APLL) for generating frequencies that are unavailable externally. For an application note on the APLL, please ask your FAE or distributor for availability.

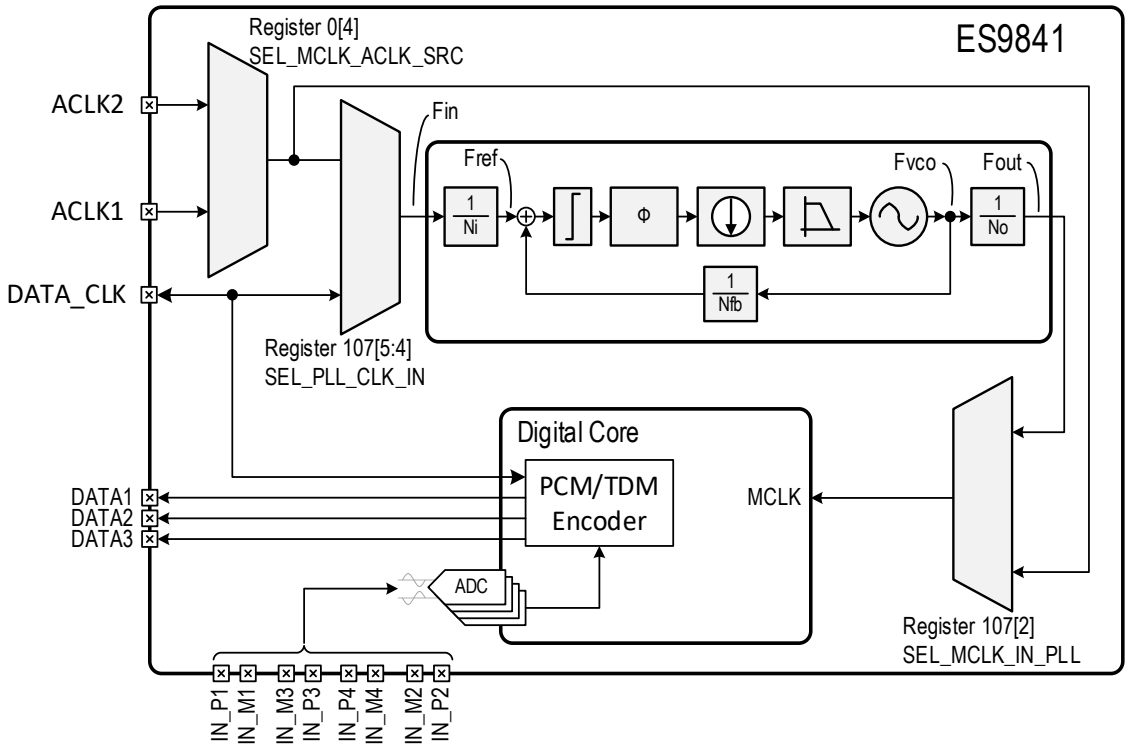


Figure 19 - Functional Block Diagram of ES9841 APLL

The input clock (F_{in}) source to the APLL is chosen between ACLK or DATA_CLK with Register 107[5:4] SEL_PLL_CLK_IN. The input MCLK source to the chip is chosen between the APLLs output or the ACLK pin with Register 107[2] SEL_MCLK_IN_PLL.

For calculation of the PLL frequency output, use the following formulas:

$$F_{ref} = \left(\frac{F_{in}}{N_i}\right) \qquad F_{vco} = \left(\frac{F_{in}}{N_i}\right) * N_{fb} \qquad N_{fb} = \frac{2^{25}}{FBDIV} \qquad F_{out} = \left(\frac{F_{in}}{N_i}\right) * \frac{N_{fb}}{N_o}$$

Where:

a. FBDIV is a 24-bit number
b. PLL frequency range requirements:
    a. Fref requirement: 2.5MHz < Fref < 13 MHz
    b. Fvco requirement: 90MHz < Fvco < 110MHz
    c. Fout requirement: 22.5792/24.576MHz & 45.1584/49.152Mhz
c. Ni = input divider
    - Accessible from Reg 113-115[8:0], PLL_CLK_IN_DIV
d. No = output divider
    - Accessible from Reg 113-115[15:12], PLL_CLK_OUT_DIV
e. Nfb = feedback divider
    - Accessible from Reg 110-112[23:0], PLL_CLK_FB_DIV
        - Note: Toggle Reg 113-115[9] PLL_FB_DIV_LOAD to load PLL_CLK_FB_DIV value

44.1kHz Base Rates (SYNC Slave Mode)							
FS (kHz)	DATA_CLK (MHz)	Ni	Fref (MHz)	FBDIV	Fvco (MHz)	No	Fout (MHz)
32-Bit Frame							
352.8	22.5792	2	11.2896	4194304	90.3168	4	22.5792
176.4	11.2896	1	11.2896	4194304	90.3168	4	22.5792
88.2	5.6448	1	5.6448	2097152	90.3168	4	22.5792
44.1	2.8224	1	2.8224	1048576	90.3168	4	22.5792
16-Bit Frame							
352.8	11.2896	1	11.2896	4194304	90.3168	4	22.5792
176.4	5.6448	1	5.6448	2097152	90.3168	4	22.5792
88.2	2.8224	1	2.8224	1048576	90.3168	4	22.5792
44.1	1.4112	1	1.4112	524288	90.3168	4	22.5792

Table 27 - APLL Divider Values for 44.1kHz Base Rates

48kHz Base Rates (SYNC Slave Mode)							
FS (kHz)	DATA_CLK (MHz)	Ni	Fref (MHz)	FBDIV	Fvco (MHz)	No	Fout (MHz)
32-Bit Frame							
384	24.576	2	12.288	4194304	98.304	4	24.576
192	12.288	1	12.288	4194304	98.304	4	24.576
96	6.144	1	6.144	2097152	98.304	4	24.576
48	3.072	1	3.072	1048576	98.304	4	24.576
16-Bit Frame							
384	12.288	1	12.288	4194304	98.304	4	24.576
192	6.144	1	6.144	2097152	98.304	4	24.576
96	3.072	1	3.072	1048576	98.304	4	24.576
48	1.536	1	1.536	524288	98.304	4	24.576

Table 28 - APLL Divider Values for 48kHz Base Rates

Note: An input bit clock to the APLL for FS = 32kHz (32kHz x 32bit x 2 channel) is unsupported.

Switching Characteristics

Parameter	Notes	Min.	Typ.	Max.	Unit
MCLK[1]					
Frequency		22.5792	-	49.152	MHz
Duty Cycle		45	-	55	%
PCM Mode[2]					
WS Frequency[3] (Word Select Clock)		MCLK/1024	-	MCLK/128	kHz
BCLK Frequency (Bit Clock)		(16*2*WS)	TDM_WORD_WIDTH)* (TDM_CH_NUM+1)*WS	MCLK	MHz
WS Frequency (Word Select Clock)	64FS Mode[4]	352.8	MCLK/64	768	kHz
BCLK Frequency (Bit Clock)		22.5792	MCLK	49.152	MHz
TDM Mode					
WS Frequency (Word Select Clock)	TDM4	MCLK/1024	-	MCLK/128	kHz
	TDM8		-	MCLK/256	kHz
	TDM16		-	MCLK/512	kHz
	TDM32		-	MCLK/1024	kHz
BCLK Frequency (Bit Clock)		(16*2*WS)	(TDM_WORD_WIDTH)* (TDM_CH_NUM+1)*WS	MCLK	MHz

Table 29 - Switching Characteristics

[1] MCLK must be synchronous to the digital audio clock.
[2] In hardware mode, only 32-bit word widths are supported for both PCM, 32-bit and 16-bit for TDM.
[3] The ES9841 supports sample rates of 32kHz only if supplied with an external synchronous 45.1584/49.152MHz or 22.5792/24.576MHz ACLK input.
[4] 64FS mode is for 705.6/768kHz with 45.1584/49.152MHz or 352.8/384kHz with 22.5792/24.576MHz.

Timing Characteristics

Bit-Clock (BCLK) and Word-Select (WS) Timing

Master Mode

For maximum flexibility the Master BCK generated can be inverted with Register 8[2] MASTER_BCK_INV and Register 8[3] MASTER_WS_INVERT respectively.

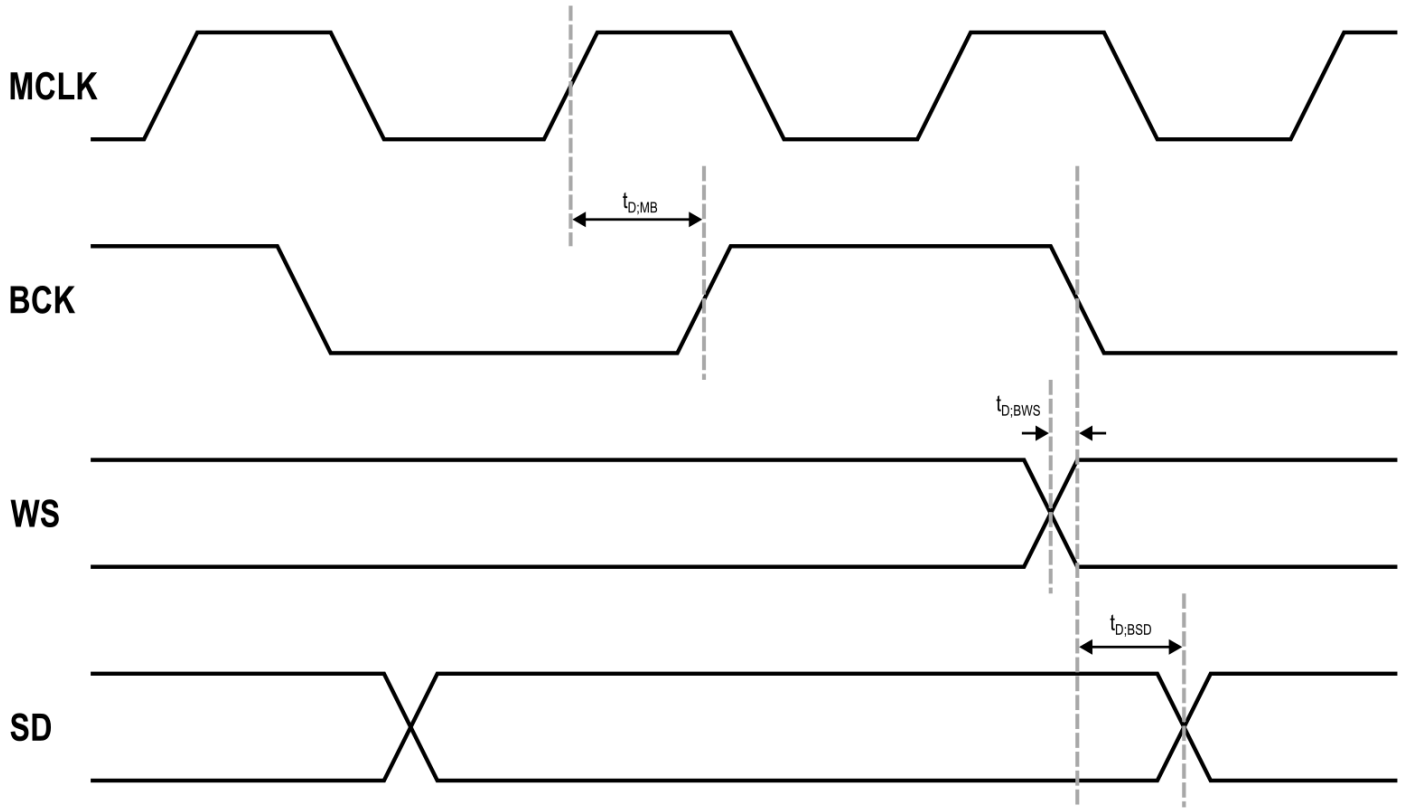


Figure 20 - Bit-Clock to Word-Select Master Mode Timing Diagram

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK-to-BCK output delay	$t_{D;MB}$	7.52	-	14.31	ns
BCK-to-WS output delay	$t_{D;BWS}$	-0.33	-	-0.15	ns
BCK-to-DATAx output delay	$t_{D;BSD}$	3.73	-	6.99	ns

Table 30 - Bit-Clock to Word-Select Master Mode Timing Numbers

Slave Mode

In this diagram SD_O is the output data lines from the PCM/TDM Encoder and SD_I is the input data for the TDM Daisy Chain. The setup and hold time for SD_I and WS are equivalent.

For maximum flexibility the input Slave BCK can be inverted with Register 8[7] SLAVE_BCK_INV.

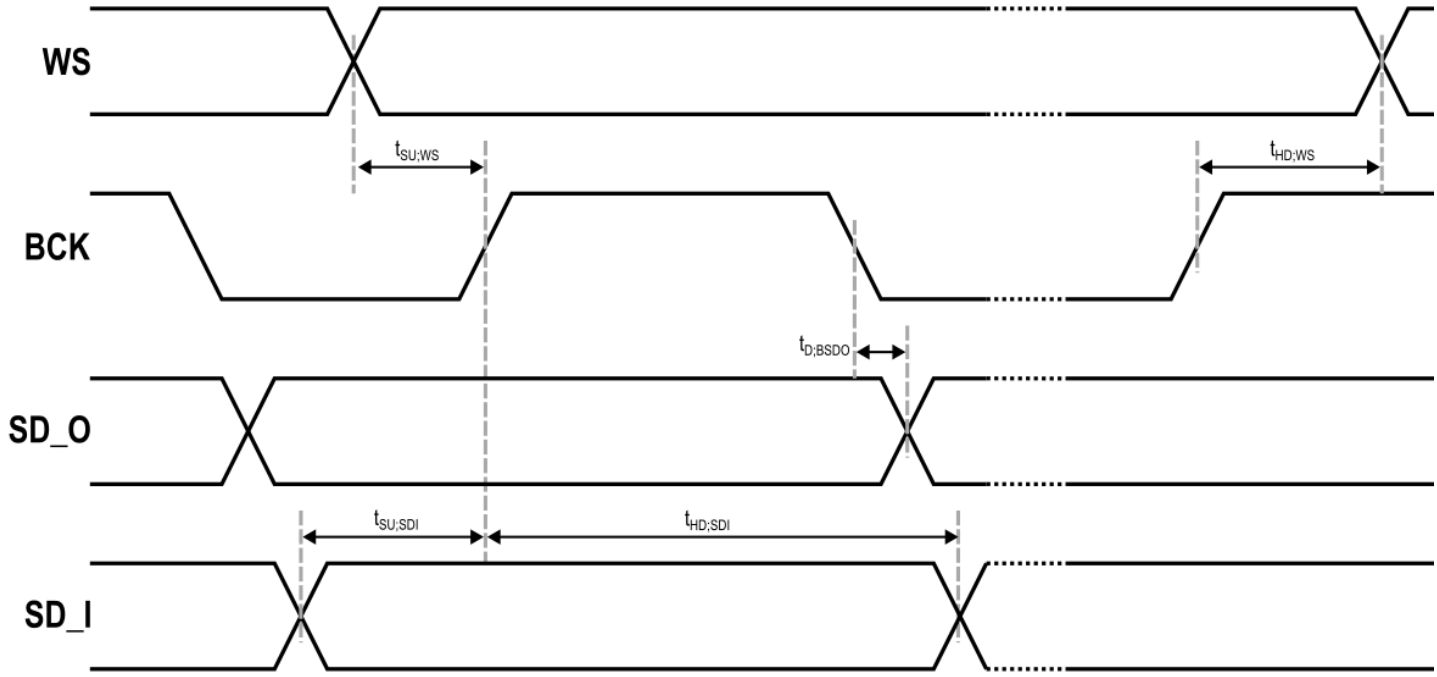


Figure 21 - Bit-Clock to Word-Select Slave Mode Timing Diagram

Parameter	Symbol	Min.	Typ.	Max.	Unit
WS setup time	$t_{SU;WS}$	0	-	-	ns
WS hold time	$t_{HD;WS}$	3	-	-	ns
DATA Input setup time	$t_{SU;SDI}$	0	-	-	ns
DATA Input hold time	$t_{HD;SDI}$	3	-	-	ns
BCK-to-DATAx output delay	$t_{D;BSDO}$	3.73	-	6.99	ns

Table 31 - Bit-Clock to Word-Select Slave Mode Timing Numbers

I²C Slave Interface Timing

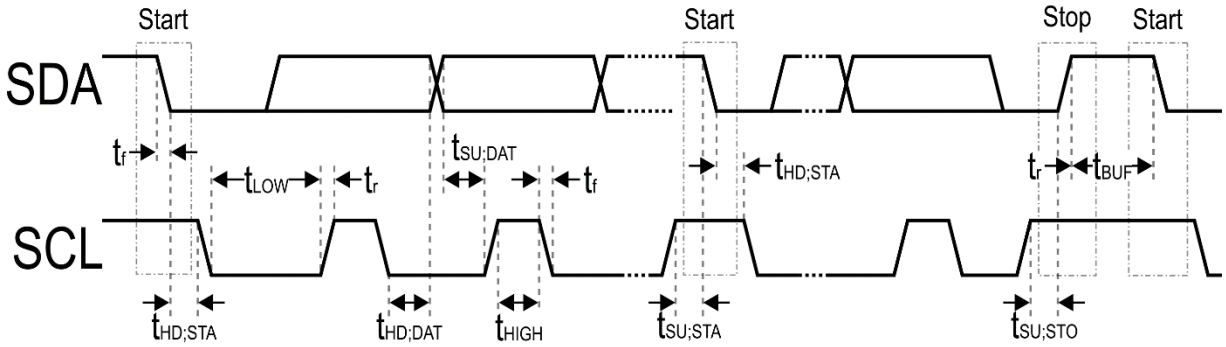


Figure 22 - I²C Slave Control Interface Timing

Parameter	Symbol	Standard-Mode			Unit
		MIN	TYP	MAX	
SCL Clock Frequency	f_{SCL}	-	-	1	MHz
START condition hold time	$t_{HD;STA}$	4	-	-	ns
LOW period of SCL	t_{LOW}	96	-	-	ns
HIGH period of SCL (>10/CLK)	t_{HIGH}	96	-	-	ns
START condition setup time (repeat)	$t_{SU;STA}$	216	-	-	ns
SDA hold time from SCL falling	$t_{HD;DAT}$	1	-	-	ns
SDA setup time from SCL rising	$t_{SU;DAT}$	180	-	-	ns
Rise time of SDA and SCL	t_r	-	180	-	ns
Fall time of SDA and SCL	t_f	18	-	-	ns
STOP condition setup time	$t_{SU;STO}$	1	-	-	ns
Bus free time between transmissions	t_{BUF}	168	-	-	ns
Capacitive load for each bus line	C_b	-	-	80	pF

Table 32 - I²C Slave/Synchronous Slave Interface Timing Definitions

SPI Slave Interface Timing

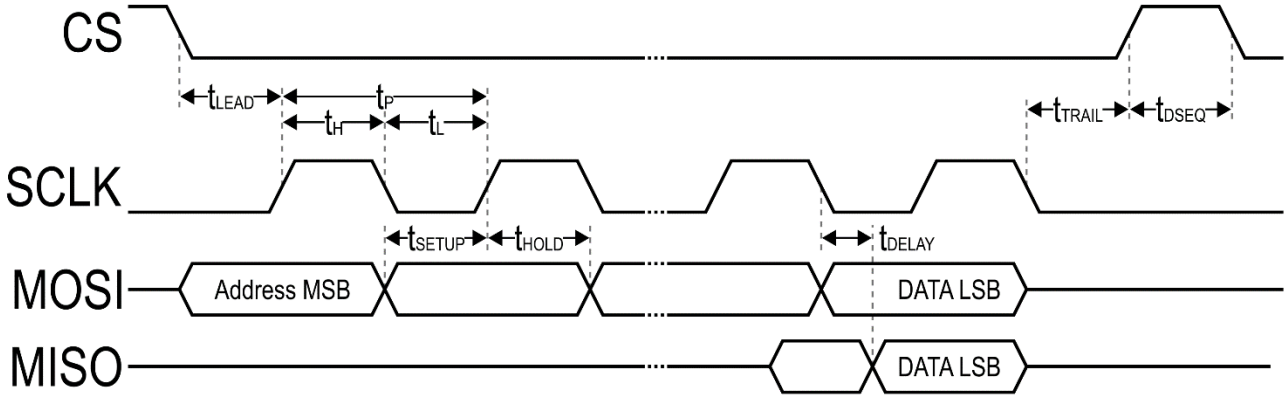


Figure 23 - SPI Slave Interface Timing

Parameter	Symbol	Min [ns]	Max [ns]
CS Lead Time (SCLK rising edge)	t_{LEAD}	2	-
CS Trail Time (SCLK falling edge)	t_{TRAIL}	2	-
MOSI Data Setup Time	t_{SETUP_MOSI}	5	-
MOSI Data Hold Time	t_{HOLD_MOSI}	7	-
SCLK-MISO Delay Time	t_{DELAY_MISO}	-	12
SCLK Period	t_{P_SCLK}	40	-
SCLK High Pulse Duration	t_{H_SCLK}	8	-
SCLK Low Pulse Duration	t_{L_SCLK}	8	-
Sequential Transfer Delay	t_{DSEQ}	40	-

Table 33 - SPI Slave Interface Timing

Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage • AVCC • AVDD • DVDD	 • -0.3V to +3.7V with respect to ground • -0.3V to +3.7V with respect to ground • -0.3V to +1.4V with respect to ground
Storage Temperature	-65ºC to +150ºC
Operating Junction Temperature	+125ºC
Voltage Range for Digital Input Pins	-0.3V to AVDD (nom) +0.3V
Maximum/Minimum Input Voltage on IN_P IN_M pins	+6V to -0.4V

Table 34 - Absolute Maximum Ratings

WARNING: Stresses beyond those listed under here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied.

ESD Ratings

ESD Standard	Rating
Human Body Model (HBM), ANSI/ESDA/JEDEC JS-001	2kV
Charge Device Model (CDM), ANSI/ESDA/JEDEC JS-002	500V

Table 35 - ESD Ratings

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

IO Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT
High-level input voltage	VIH	(AVDD / 2) + 0.2		V
Low-level input voltage	VIL		1.61	V
High-level output voltage	VOH	AVDD – 0.2		V
Low-level output voltage	VOL		0.2	V

Table 36 - I/O Electrical Characteristics

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Operating Temperature	T_A	-20°C to +85°C
AVCC		+3.3V ±5%
AVDD		+3.3V ±5%
VREF_BUF_R		Internal (+2.85V)
VREF_BUF_L		Internal (+2.85V)
DVDD		Internal (+1.2V)

Table 37 - Recommended Operating Conditions

Recommended Power Up/Down Sequence

The recommended power up sequence for the ES9841, the AVDD supply is enabled ~200us before AVCC. All supplies should be stable before CHIP_EN is asserted. There is a ~20ms delay between enabling the ADCs and valid data output. MCLK must be on before enabling the ADCs.

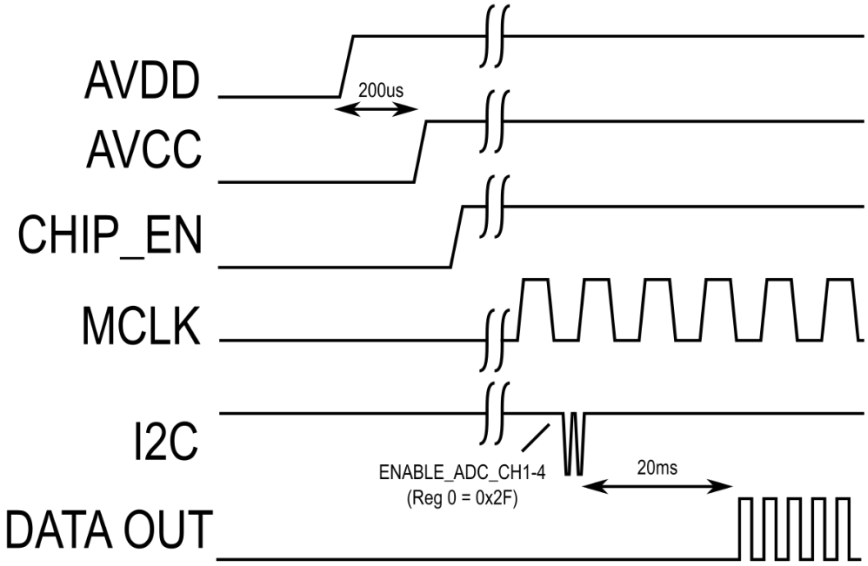


Figure 24 - Recommended Power Up Sequence

On power down, the order to shut off is MCLK & CHIP_EN, AVCC which must be before AVDD.

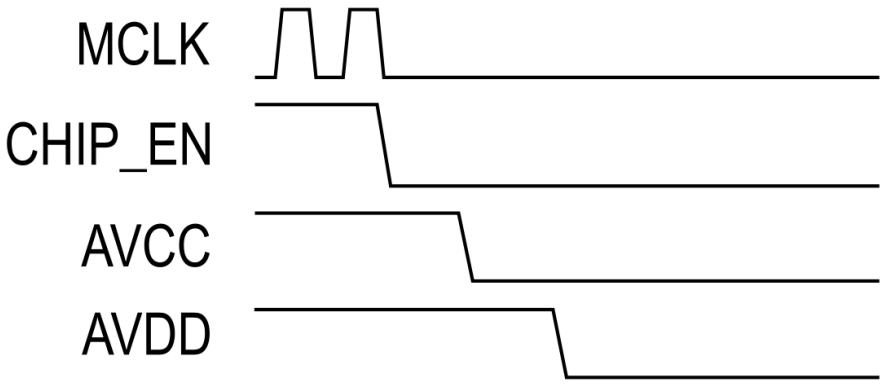


Figure 25 - Recommended Power Down Sequence

Power Consumption

Test Conditions (unless otherwise noted)
T_A = 25ºC, AVCC = AVDD = +3.3V, 1kHz sine wave signal. AVDD supply includes DVDD current.

Parameter	Min	Typ.	Max	Unit
Standby (CHIP_EN=0)				
AVCC_3V3		<0.1		µA
AVDD		<0.3		µA
Total Power Consumption		**<2**		**µW**
MCLK = 49.152MHz				
48kHz 2ch Slave PCM				
AVCC_3V3		28		mA
AVDD		19		mA
Total Power Consumption		**155**		**mW**
192kHz 2ch Slave PCM				
AVCC_3V3		28		mA
AVDD		28		mA
Total Power Consumption		**185**		**mW**
MCLK = 24.576MHz				
48kHz 2ch Slave PCM				
AVCC_3V3		28		mA
AVDD		17		mA
Total Power Consumption		**148**		**mW**
192kHz 2ch Slave PCM				
AVCC_3V3		28		mA
AVDD		26		mA
Total Power Consumption		**178**		**mW**

Table 38 - Power Consumption

Performance

Test Conditions (unless otherwise noted). Measured on ES9841 2v0 Evaluation Board.
T_A = 25ºC, AVCC = AVDD = +3.3V, fs = 48kHz, MCLK = 49.152MHz from powered oscillator, PCM output, differential input.t.

Dynamic Performance						
Parameter			**Min**	**Typ**	**Max**	**Unit**
Resolution				32		Bit
Fs = 48kHz, BW = AC(<10Hz) - Fs/2						
THD+N Ratio @ 1kHz, -1dBFS output	4 ch mode			-115		dB
	2 ch mode	STEREO_MODE=1				dB
Fs = 96kHz, BW = AC(<10Hz) - Fs/2						
THD+N Ratio @ 1kHz, -1dBFS output	4 ch mode			-112		dB
	2 ch mode	STEREO_MODE=1				dB
Fs = 192kHz, BW = AC(<10Hz) - Fs/2						
THD+N Ratio @ 1kHz, -1dBFS output	4 ch mode			-109		dB
	2 ch mode	STEREO_MODE=1				dB
True DNR						
True DNR A-weighted	4 ch mode			122		dBFS
	2 ch mode	STEREO_MODE=1		125		dBFS

Table 39 - Performance

Analog Input					
Parameter		**Min**	**Typ**	**Max**	**Unit**
Input Impedance	Per Input Pin		833 ± 15%		Ω
Input DC Common Mode			VREF_BUF_L/2 VREF_BUF_R/2		Vdc
Input Amplitude for Digital Full Scale Output	Per Input pin		V_REF_BUF_L / (2*√2)		Vrms
	Differential (IN_Px to IN_Mx)		V_REF_BUF_L / √2		Vrms

Table 40 – Analog Input Characteristics

Register Overview

A system clock is not required to access registers.

Read/Write Register Addresses

Registers 0-123 (0x00 - 0x7B) are read and write registers.

Read-Only Register Addresses

Register 224-247 (0xE0 - 0xF7) are read only registers.

Multi-Byte Registers

Multi-Byte registers must be written from LSB to MSB. Data is latched when MSB is written.
Multi-Byte registers must be read from LSB to MSB. Data is latched when LSB is read.
MSB is always stored in the highest register address.

Register Map

Addr (Hex)	Addr (Dec)	Register	7	6	5	4	3	2	1	0
0x00	0	SYS CONFIG	SOFT_RESET	RESERVED	EN_MCLK_IN	SEL_MCLK_ ACLK_SRC	ENABLE_ADC_ CH4	ENABLE_ADC_ CH3	ENABLE_ADC_ CH2	ENABLE_ADC_ CH1
0x01	1	FS CONFIG	RESERVED		STEREO_MODE	MONO_MODE	RESERVED	ENABLE_64FS_ MODE	AUTO_FS_ DETECT_ BLOCK_64FS	AUTO_FS_ DETECT
0x02	2	ENCODER CONFIG	RESERVED			ENABLE_SPDIF _ENCODE	RESERVED			ENABLE_TDM_ ENCODE
0x03	3	OUTPUT SELECT	RESERVED	OUTPUT_SEL			RESERVED			ENABLE_PDM_ MIC_DECODE
0x04	4	FRONT-END CLOCK CONTROL	RESERVED	MCLK_128FS_ HALF_DIV	MCLK_128FS_DIV					
0x05	5	BACK-END CLOCK CONTROL	RESERVED			MCLK_24M_ DIV2	RESERVED			
0x06	6	MASTER CLK CONFIG	MASTER_DCLK_DIV							
0x07	7	MISC CLOCK CONFIG	RESERVED				ENABLE_WS_ MONITOR	ENABLE_BCK_ MONITOR	FORCE_PLL_LO CK	CLK_FAULT_ DET_EN
0x08	8	MASTER MODE CONFIG	SLAVE_BCK_ INVERT	RESERVED	MASTER_WS_ CLK_PHASE	MASTER_WS_ PULSE_MODE	MASTER_WS_ INVERT	MASTER_BCK_ INVERT	RESERVED	PCM_MASTER_ MODE_EN
0x09	9	TDM CONFIG 1	RESERVED	AUTO_CH_ DETECT	RESERVED	TDM_CH_NUM				
0x0A	10	TDM CONFIG 2	RESERVED	NOISE_FLOOR_ SHAPE_16BIT	TDM_WORD_WIDTH		TDM_BIT_DEPTH		TDM_VALID_ EDGE	TDM_LJ
0x0B	11	TDM ENC CH1 SLOT CONFIG	RESERVED	TDM_ENC_LINE_SEL_CH1		TDM_ENC_SLOT_SEL_CH1				
0x0C	12	TDM ENC CH2 SLOT CONFIG	RESERVED	TDM_ENC_LINE_SEL_CH2		TDM_ENC_SLOT_SEL_CH2				
0x0D	13	TDM ENC CH3 SLOT CONFIG	RESERVED	TDM_ENC_LINE_SEL_CH3		TDM_ENC_SLOT_SEL_CH3				
0x0E	14	TDM ENC CH4 SLOT CONFIG	RESERVED	TDM_ENC_LINE_SEL_CH4		TDM_ENC_SLOT_SEL_CH4				
0x0F	15	TDM ENC DAISY CHAIN	TDM_ENC_ DAISY_CHAIN	RESERVED	TDM_DAISYLIN E_SEL	TDM_ENC_DATA_LATCH_ADJ				
0x10-0x14	16-20	RESERVED	RESERVED							
0x15	21	PDM I/O CONFIG	PDM_MIC_ INPUT_SEL_ CH34	PDM_MIC_ INPUT_SEL_ CH12	PDM_MIC_ INPUT_SAMPLE _EDGE	PDM_MIC_ INPUT_DATA_ PHASE	RESERVED			
0x16	22	PDM CLK DIVIDER	RESERVED	PDM_CLK_DIV						
0x17	23	S/PDIF DATA SELECT	RESERVED						SPDIF_CH_ PAIR_SEL	RESERVED
0x18	24	S/PDIF CS ADDR	SPDIF_CS_WE	RESERVED				SPDIF_CS_BYTE_ADDR		
0x19	25	S/PDIF CS DATA	SPDIF_CS_BYTE_DATA							
0x1A-0x1F	26-31	RESERVED	RESERVED							
0x20	32	STATUS BITS MASK	MASK_ADC_ OVERLOAD_ CH4	MASK_ADC_ OVERLOAD_ CH3	MASK_ADC_ OVERLOAD_ CH2	MASK_ADC_ OVERLOAD_ CH1	MASK_PEAK_ DET_CH4	MASK_PEAK_ DET_CH3	MASK_PEAK_ DET_CH2	MASK_PEAK_ DET_CH1
0x21	33	STATUS BITS CLEAR	CLEAR_ADC_ OVERLOAD_ CH4	CLEAR_ADC_ OVERLOAD_ CH3	CLEAR_ADC_ OVERLOAD_ CH2	CLEAR_ADC_ OVERLOAD_ CH1	CLEAR_PEAK_ DET_CH4	CLEAR_PEAK_ DET_CH3	CLEAR_PEAK_ DET_CH2	CLEAR_PEAK_ DET_CH1
0x22-0x2E	34-46	RESERVED	RESERVED							
0x2F	47	GPIO1/2 CONFIG	GPIO2_CFG				GPIO1_CFG			
0x30	48	GPIO3/4 CONFIG	GPIO4_CFG				GPIO3_CFG			
0x31	49	GPIO5/6 CONFIG	GPIO6_CFG				GPIO5_CFG			
0x32	50	GPIO7/8 CONFIG	GPIO8_CFG				GPIO7_CFG			
0x33	51	GPIO9/10 CONFIG	GPIO10_CFG				GPIO9_CFG			
0x34	52	GPIO11 CONFIG	RESERVED				GPIO11_CFG			
0x35	53	GPIO INPUT ENABLE	GPIO8_IE	GPIO7_IE	GPIO6_IE	GPIO5_IE	GPIO4_IE	GPIO3_IE	GPIO2_IE	GPIO1_IE
0x36	54		RESERVED					GPIO11_IE	GPIO10_IE	GPIO9_IE
0x37	55	GPIO OUTPUT ENABLE	GPIO8_OE	GPIO7_OE	GPIO6_OE	GPIO5_OE	GPIO4_OE	GPIO3_OE	GPIO2_OE	GPIO1_OE
0x38	56		RESERVED					GPIO11_OE	GPIO10_OE	GPIO9_OE
0x39	57	GPIO INVERT	GPIO8_INV	GPIO7_INV	GPIO6_INV	GPIO5_INV	GPIO4_INV	GPIO3_INV	GPIO2_INV	GPIO1_INV
0x3A	58		RESERVED					GPIO11_INV	GPIO10_INV	GPIO9_INV
0x3B	59	GPIO WEAK KEEPER	GPIO8_WK_EN	GPIO7_WK_EN	GPIO6_WK_EN	GPIO5_WK_EN	GPIO4_WK_EN	GPIO3_WK_EN	GPIO2_WK_EN	GPIO1_WK_EN
0x3C	60		RESERVED					GPIO11_WK_EN	GPIO10_WK_EN	GPIO9_WK_EN
0x3D	61	GPIO READ	GPIO8_READ	GPIO7_READ	GPIO6_READ	GPIO5_READ	GPIO4_READ	GPIO3_READ	GPIO2_READ	GPIO1_READ
0x3E	62		RESERVED					GPIO11_READ	GPIO10_READ	GPIO9_READ
0x3F	63	DETECTION FLAG CONFIG	LIVE_DETECT_ CH4	LIVE_DETECT_ CH3	LIVE_DETECT_ CH2	LIVE_DETECT_ CH1	DETECT_FLAG_ SEL_CH4	DETECT_FLAG_ SEL_CH3	DETECT_FLAG_ SEL_CH2	DETECT_FLAG_ SEL_CH1
0x40	64	PWM1 COUNT	PWM1_COUNT							
0x41	65	PWM1 FREQUENCY	PWM1_FREQ							
0x42	66		PWM1_FREQ							
0x43	67	PWM2 COUNT	PWM2_COUNT							
0x44	68	PWM2 FREQUENCY	PWM2_FREQ							
0x45	69		PWM2_FREQ							
0x46	70	PWM3 COUNT	PWM3_COUNT							
0x47	71	PWM3 FREQUENCY	PWM3_FREQ							
0x48	72		PWM3_FREQ							
0x49	73	ADC NEGATION	RESERVED				ADC_NEG_SEL _CH4	ADC_NEG_SEL _CH3	ADC_NEG_SEL _CH2	ADC_NEG_SEL _CH1
0x4A	74	ADC FIR FILTER	FILTER_SHAPE			BYPASS_FIR2X	BYPASS_FIR4X	BYPASS_IIR		
0x4B	75	RESERVED	RESERVED							
0x4C	76	DC BLOCKING	DC_BLOCK_EN _CH4	DC_BLOCK_EN _CH3	DC_BLOCK_EN _CH2	DC_BLOCK_EN _CH1	RESERVED			
0x4D-0x50	77-80	RESERVED	RESERVED							
0x51	81	VOLUME CH1	VOLUME_CH1							
0x52	82	VOLUME CH2	VOLUME_CH2							
0x53	83	VOLUME CH3	VOLUME_CH3							
0x54	84	VOLUME CH4	VOLUME_CH4							
0x55	85	DIGITAL GAIN	RESERVED	DIGITAL_GAIN_CH2			RESERVED	DIGITAL_GAIN_CH1		
0x56	86		MONO_ VOLUME	DIGITAL_GAIN_CH4			RESERVED	DIGITAL_GAIN_CH3		

0x57	87	PHASE INVERSION	RESERVED				VOL_PHASE_INV_CH4	VOL_PHASE_INV_CH3	VOL_PHASE_INV_CH2	VOL_PHASE_INV_CH1
0x58	88	VOLUME UP RAMP RATE	VOL_RAMP_RATE_UP							
0x59	89	VOLUME DOWN RAMP RATE	VOL_RAMP_RATE_DOWN							
0x5A	90	THD COMP C2 CH1/2	THD_COMP_C2_CH12							
0x5B	91		THD_COMP_C2_CH12							
0x5C	92	THD COMP C3 CH1/2	THD_COMP_C3_CH12							
0x5D	93		THD_COMP_C3_CH12							
0x5E	94	THD COMP C2 CH3/4	THD_COMP_C2_CH34							
0x5F	95		THD_COMP_C2_CH34							
0x60	96	THD COMP C3 CH3/4	THD_COMP_C3_CH34							
0x61	97		THD_COMP_C3_CH34							
0x62	98	PEAK DETECT ENABLE	RESERVED				PEAK_DETECT_EN_CH4	PEAK_DETECT_EN_CH3	PEAK_DETECT_EN_CH2	PEAK_DETECT_EN_CH1
0x63	99	PEAK DETECT CONFIG	RESERVED	LOCK_PEAK_VALUE	RESERVED	PEAK_DECAY_RATE				
0x64	100	PEAK THRESHOLDS	PEAK_THRESH_CH1							
0x65	101		PEAK_THRESH_CH2							
0x66	102		PEAK_THRESH_CH3							
0x67	103		PEAK_THRESH_CH4							
0x68-0x6A	104-106	RESERVED	RESERVED							
0x6B	107	PLL CLOCK SELECT	RESERVED	PLL_CLK_PHASE_INV	SEL_PLL_CLK_IN		EN_PLL_CLK_IN	SEL_MCLK_IN_PLL	RESERVED	
0x6C	108	PLL VCO & CP	RESERVED	PLL_CP_BIAS_SEL			PLL_CP_EN	PLL_VCO_EN	PLL_CLKSMP_EN	PLL_DIG_RSTB
0x6D	109	PLL REGULATOR	RESERVED				PLL_REG_EN	PLL_REG_LN	RESERVED	
0x6E	110	PLL FEEDBACK DIV	PLL_CLK_FB_DIV							
0x6F	111		PLL_CLK_FB_DIV							
0x70	112		PLL_CLK_FB_DIV							
0x71	113	PLL IN & OUT DIV	PLL_CLK_IN_DIV							
0x72	114		PLL_CLK_OUT_DIV				RESERVED		PLL_FB_DIV_LOAD	PLL_CLK_IN_DIV
0x73	115		RESERVED		PLL_CLK_OUT_DIV_PHASE_EN		RESERVED			
0x74-0x79	116-121	RESERVED	RESERVED						VCO_IB_AMP_CTRL	
0x7A	122	SPI MASTER CONFIG	SPI_M_PULSE_WIDTH				SPI_M_EN	SPI_M_MODE	SPI_M_SEND_BYTE	SPI_M_START
0x7B	123	SPI MASTER DATA OUT	SPI_M_DATA_O							
0xE0	224	VALIDITY READ	PLL_LOCKED	RESERVED	TDM_ENC_VALID	AUTO_CH_NUM				
0xE1	225	CHIP ID	CHIP_ID							
0xE2-0xE5	226-229	RESERVED	RESERVED							
0xE6	230	AUTO FS READ	EN_64FS_MODE_AUTO	MCLK_128FS_HALF_DIV_AUTO	MCLK_128FS_DIV_AUTO					
0xE7	231	CLOCK VALIDITY	RESERVED					RATIO_VALID	BCK_INVALID	WS_INVALID
0xE8	232	GPIO READBACK	GPIO8_R	GPIO7_R	GPIO6_R	GPIO5_R	GPIO4_R	GPIO3_R	GPIO2_R	GPIO1_R
0xE9	233		RESERVED					GPIO11_R	GPIO10_R	GPIO9_R
0xEA	234	ADC OVERLOAD FLAGS	ADC_OVERLOAD_FLAG_CH4	ADC_OVERLOAD_FLAG_CH3	ADC_OVERLOAD_FLAG_CH2	ADC_OVERLOAD_FLAG_CH1	ADC_OVERLOAD_FLAG_LAT_CH4	ADC_OVERLOAD_FLAG_LAT_CH3	ADC_OVERLOAD_FLAG_LAT_CH2	ADC_OVERLOAD_FLAG_LAT_CH1
0xEB	235	PEAK FLAGS	PEAK_FLAG_CH4	PEAK_FLAG_CH3	PEAK_FLAG_CH2	PEAK_FLAG_CH1	PEAK_FLAG_LAT_CH4	PEAK_FLAG_LAT_CH3	PEAK_FLAG_LAT_CH2	PEAK_FLAG_LAT_CH1
0xEC	236	PEAK CH1 READ	PEAK_LEVEL_CH1							
0xED	237		PEAK_LEVEL_CH1							
0xEE	238	PEAK CH2 READ	PEAK_LEVEL_CH2							
0xEF	239		PEAK_LEVEL_CH2							
0xF0	240	PEAK CH3 READ	PEAK_LEVEL_CH3							
0xF1	241		PEAK_LEVEL_CH3							
0xF2	242	PEAK CH4 READ	PEAK_LEVEL_CH4							
0xF3	243		PEAK_LEVEL_CH4							
0xF4-0xF6	244-246	RESERVED	RESERVED							
0xF7	247	SPI MASTER DATA IN	SPI_M_DATA_I							

Table 41 - Register Map

Register Listing

System Registers

Register 0: SYS CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b1	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RESET	Performs soft reset to digital core, resetting registers to their power-on defaults. Note: When performing a Soft Reset write 0xA0 to Register 0 to ensure EN_MCLK_IN = 1'b1.
[6]	RESERVED	N/A
[5]	EN_MCLK_IN	Enables clock inputs to the digital core. • 1'b0: Disabled • 1'b1: Enabled (default)
[4]	SEL_MCLK_ACLK_SRC	Selects which ACLK source is used by the digital core and analog ADC, when EN_MCLK_IN is set. • 1'b0: ACLK1 (default) • 1'b1: ACLK2
[3]	ENABLE_ADC_CH4	Enables the ADC CH4 decimation path. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[2]	ENABLE_ADC_CH3	Enables the ADC CH3 decimation path. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[1]	ENABLE_ADC_CH2	Enables the ADC CH2 decimation path. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[0]	ENABLE_ADC_CH1	Enables the ADC CH1 decimation path. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled

Register 1: FS CONFIG

Bits	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	2'b00	1'b0	1'b0	1'd0	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	STEREO_MODE	Enables stereo mode, CH1 and CH3 are summed, CH2 and CH4 are summed. • 1'b0: Disabled (default) • 1'b1: Enabled
[4]	MONO_MODE	Enables mono mode, input of all channels are mixed into CH1. • 1'b0: Disabled (default) • 1'b1: Enabled
[3]	RESERVED	N/A
[2]	ENABLE_64FS_MODE	Enables 64FS mode for 768k sample rate. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	AUTO_FS_DETECT_BLOCK_64FS	Block AUTO_FS_DETECT from transitioning to 64FS mode when the detected MCLK/MCLK_128FS ratio is 64. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	AUTO_FS_DETECT	Automatically determine optimal MCLK/MCLK_128FS ratio, from detected FS. • 1'b0: Disabled, use MCLK_128FS_DIV to set ratio. • 1'b1: Enabled, overrides MCLK_128FS_DIV (default)

Register 2: ENCODER CONFIG

Bits	[7:5]	[4]	[3:1]	[0]
Default	3'd0	1'b0	3'd0	1'b1

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4]	ENABLE_SPDIF_ENCODE	Enables the S/PDIF encoding clock. • 1'b0: Disabled (default) • 1'b1: Enabled
[3:1]	RESERVED	N/A
[0]	ENABLE_TDM_ENCODE	Enables the PCM/TDM encoding clock. • 1'b0: Disabled • 1'b1: Enabled (default)

Register 3: OUTPUT SELECT

Bits	[7]	[6:4]	[3:1]	[0]
Default	1'd0	3'd0	3'd0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:4]	OUTPUT_SEL	Select which digital output to use. • 3'd0: PCM (default) • 3'd1: TDM • 3'd2-4: Reserved • 3'd5: S/PDIF • 3'd6-7: Reserved
[3:1]	RESERVED	N/A
[0]	ENABLE_PDM_MIC_DECODE	Enables PDM Microphone decoding clock. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 4: FRONT-END CLOCK CONTROL

Bits	[7]	[6]	[5:0]
Default	1'd0	1'b0	6'd3

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	MCLK_128FS_HALF_DIV	• 1'b0: Divide by SELECT_ADC_NUM + 1 (default) • 1'b1: Divide by half of SELECT_ADC_NUM + 1 Note: Can only produce half of an odd number divide
[5:0]	MCLK_128FS_DIV	Whole number divide value + 1 for MCLK_128FS (MCLK/divide_value). • 6'd0: Whole number divide value + 1 = 1 • 6'd3: Whole number divide value + 1 = 4 (default)

Register 5: BACK-END CLOCK CONTROL

Bits	[7:5]	[4]	[3:0]
Default	3'b010	1'b0	4'b1000

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4]	MCLK_24M_DIV2	Sets the rate of MCLK_24M as well as the analog ADC_CLK, relative to MCLK. Both clocks must be running at 22.5792 MHz or 24.576 MHz. • 1'b0: Rate = MCLK (default) • 1'b1: Rate = MCLK/2
[3:0]	RESERVED	N/A

Register 6: MASTER CLK CONFIG

Bits	[7:0]
Default	8'd7

Bits	Mnemonic	Description
[7:0]	MASTER_DCLK_DIV	Master mode DCLK and WS generation clock divider. Whole number divide value + 1 for MCLK_BCK_WS_GEN (MCLK/divide_value).

Register 7: MISC CLOCK CONFIG

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	4'b0100	1'b1	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	ENABLE_WS_MONITOR	Enable WS monitor, used to detect the validity of the WS signal. WS is considered invalid if BCK/WS > 1024. • 1'b0: Disabled • 1'b1: Enabled (default)
[2]	ENABLE_BCK_MONITOR	Enable BCK monitor, used to detect the validity of the BCK signal. BCK is considered invalid if MCLK/BCK > 256. • 1'b0: Disabled • 1'b1: Enabled (default)
[1]	FORCE_PLL_LOCK	Clock locking status control with PLL_LOCKED. • 1'b0: clock locking status is determined by PLL_LOCKED • 1'b1: Ignore PLL_LOCKED signal, set lock status to 1'b1
[0]	CLK_FAULT_DET_EN	Enable the clock detection circuit, sets the CLK_AVALID signal. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 8: MASTER MODE CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'd0	1'b1	1'b0	1'b0	1'b1	1'd0	1'b0

Bits	Mnemonic	Description
[7]	SLAVE_BCK_INVERT	Inverts the BCK input on DATA_CLK. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[6]	RESERVED	N/A
[5]	MASTER_WS_CLK_PHASE	Determines the BCK edge DATA_WS (DATA1) is output on, in master mode. • 1'b0: Negative edge • 1'b1: Positive edge (default) Note: MASTER_BCK_INVERT inverts this logic.
[4]	MASTER_WS_PULSE_MODE	When enabled, master WS is a 1 BCK pulse signal instead of a 50% duty cycle signal. • 1'b0: 50% duty cycle WS signal (default) • 1'b1: Pulse WS signal
[3]	MASTER_WS_INVERT	Inverts master WS output on DATA1. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[2]	MASTER_BCK_INVERT	Inverts master BCK output on DATA_CLK. • 1'b0: Non-inverted • 1'b1: Inverted (default)
[1]	RESERVED	N/A
[0]	PCM_MASTER_MODE_EN	Enables PCM master mode, generating BCK and WS. • 1'b0: Disabled, slave mode (default) • 1'b1: Enabled

Register 9: TDM CONFIG 1

Bits	[7]	[6]	[5]	[4:0]
Default	1'b0	1'b0	1'b0	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	AUTO_CH_DETECT	Automatically determine the number of TDM channels in a sample, based on the BCK/WS ratio. • 1'b0: Disabled, use TDM_CH_NUM to set channels (default) • 1'b1: Enabled, overrides TDM_CH_NUM Note: Only active in TDM slave mode.
[5]	RESERVED	N/A
[4:0]	TDM_CH_NUM	Sets number of TDM channels in each frame. • 5'd0: 1 channel • 5'd1: 2 channels (default) • 5'd31: 32 channels

Register 10: TDM CONFIG 2

Bits	[7]	[6]	[5:4]	[3:2]	[1]	[0]
Default	1'd0	1'b0	2'b00	2'b00	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	NOISE_FLOOR_SHAPE_16BIT	Sets the shape of the 16-bit PCM/TDM noise floor • 1'b0: 1st order shaping (default) • 1'b1: Flat shaping
[5:4]	TDM_WORD_WIDTH	Sets the width, in bits, of one data word / subframe. A subframe is a frame divided by the number of channels. • 2'b00: 32-bits (default) • 2'b01: 24-bits • 2'b10: 16-bits
[3:2]	TDM_BIT_DEPTH	Sets the bit depth, number of data bits, in one data word / subframe. • 2'b00: 32-bit (default) • 2'b01: 24-bit • 2'b10: 16-bit
[1]	TDM_VALID_EDGE	Sets which WS edge the frame starts on. • 1'b0: Frame starts on negedge of WS (default) • 1'b1: Frame starts on posedge of WS
[0]	TDM_LJ	Sets left-justified mode. • 1'b0: One BCK period delay (default) • 1'b1: Left-justified

Register 11: TDM ENC CH1 SLOT CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'd0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_ENC_LINE_SEL_CH1	CH1 data line selection. • 2'd0: DATA2 (default) • 2'd1: DATA3 • 2'd2: DATA4 • 2'd3: DATA5
[4:0]	TDM_ENC_SLOT_SEL_CH1	Selects which TDM channel slot is filled by the CH1 data. • 5'd0: Slot 1 (default) • 5'd31: Slot 32

Register 12: TDM ENC CH2 SLOT CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'd0	2'd0	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_ENC_LINE_SEL_CH2	CH2 data line selection. • 2'd0: DATA2 (default) • 2'd1: DATA3 • 2'd2: DATA4 • 2'd3: DATA5
[4:0]	TDM_ENC_SLOT_SEL_CH2	Selects which TDM channel slot is filled by the CH2 data. • 5'd0: Slot 1 • 5'd1: Slot 2 (default) • 5'd31: Slot 32

Register 13: TDM ENC CH3 SLOT CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'd0	2'd1	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_ENC_LINE_SEL_CH3	CH3 data line selection. • 2'd0: DATA2 • 2'd1: DATA3 (default) • 2'd2: DATA4 • 2'd3: DATA5
[4:0]	TDM_ENC_SLOT_SEL_CH3	Selects which TDM channel slot is filled by the CH3 data. • 5'd0: Slot 1 (default) • 5'd31: Slot 32

Register 14: TDM ENC CH4 SLOT CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'd0	2'd1	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_ENC_LINE_SEL_CH4	CH4 data line selection. • 2'd0: DATA2 • 2'd1: DATA3 (default) • 2'd2: DATA4 • 2'd3: DATA5
[4:0]	TDM_ENC_SLOT_SEL_CH4	Selects which TDM channel slot is filled by the CH4 data. • 5'd0: Slot 1 • 5'd1: Slot 2 (default) • 5'd31: Slot 32

Register 15: TDM ENC DAISY CHAIN

Bits	[7]	[6]	[5]	[4:0]
Default	1'b0	1'd0	1'b0	5'd0

Bits	Mnemonic	Description
[7]	TDM_ENC_DAISY_CHAIN	TDM encoder daisy chain mode. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	RESERVED	N/A
[5]	TDM_DAISYLINE_SEL	Daisy chain output data line selection, chains the data from DATA3/GPIO4 onto: • 1'b0: DATA2 (default) • 1'b1: DATA5/GPIO6
[4:0]	TDM_ENC_DATA_LATCH_ADJ	Adjusts the position of the MSB within each TDM slot by TDM_ENC_DATA_LATCH_ADJ clock cycles. ADC data is placed ahead of the normal position. • 5'd0: Normal position • 5'd1-31: Data is placed ADC_TDM_DATA_LATCH_ADJ BCKs ahead

Register 20-16: RESERVED

Register 21: PDM I/O CONFIG

Bits	[7]	[6]	[5]	[4]	[3:0]
Default	1'b0	1'b0	1'b1	1'b0	4'd0

Bits	Mnemonic	Description
[7]	PDM_MIC_INPUT_SEL_CH34	Selects the PDM microphone input to the CH3 and CH4 datapaths. • 1'b0: Analog input to datapath (default) • 1'b1: PDM microphone input to datapath
[6]	PDM_MIC_INPUT_SEL_CH12	Selects the PDM microphone input to the CH1 and CH2 datapaths. • 1'b0: Analog input to datapath (default) • 1'b1: PDM microphone input to datapath
[5]	PDM_MIC_INPUT_SAMPLE_EDGE	Sets the edge of PDM_CLK where the PDM microphone input sample increments. • 1'b0: Rising edge • 1'b1: Falling edge (default)
[4]	PDM_MIC_INPUT_DATA_PHASE	Selects the CH input edges of the PDM microphone input. • 1'b0: CH1 on the rising edge of PDM_CLK, CH2 on the falling edge (default) • 1'b1: CH2 on the rising edge of PDM_CLK, CH1 on the falling edge
[3:0]	RESERVED	N/A

Register 22: PDM CLK DIVIDER

Bits	[7]	[6:0]
Default	1'b0	7'd3

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:0]	PDM_CLK_DIV	Frequency divider for the PDM microphone clock, PDM_CLK. Overidden by AUTO_FS_DETECT, sets PDM_CLK_DIV = MCLK_128FS_DIV_AUTO[3:0]. • 7'd0: 2 * (PDM_CLK_DIV + 1) = DIV2 • 7'd3: 2 * (PDM_CLK_DIV + 1) = DIV8 (default) $\text{PDM\_CLK [Hz]} = \frac{\text{MCLK}}{2 \cdot (\text{PDM\_CLK\_DIV} + 1)}$

Register 23: S/PDIF DATA SELECT

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b0	1'd0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	SPDIF_CH_PAIR_SEL	Selects which channel pair is sent to the S/PDIF encoder. • 1'b0: CH1/2 (default) • 1'b1: CH3/4
[0]	RESERVED	N/A

Register 24: S/PDIF CS ADDR

Bits	[7]	[6:3]	[2:0]
Default	1'b0	4'd0	3'd0

Bits	Mnemonic	Description
[7]	SPDIF_CS_WE	Write enable for the S/PDIF channel status bits. Writes the SPDIF_CS_DATA to the byte at address SPDIF_CS_BYTE_SEL. Toggle high-low to perform a write.
[6:3]	RESERVED	N/A
[2:0]	SPDIF_CS_BYTE_ADDR	Byte of the 40-bit S/PDIF Channel Status to write to.

Register 25: S/PDIF CS DATA

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	SPDIF_CS_BYTE_DATA	Data to write into the 40-bit S/PDIF Channel Status.

Register 31-26: RESERVED

Register 32: STATUS BITS MASK

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	MASK_ADC_OVERLOAD_CH4	Masks the latched ADC_OVERLOAD status bit on ADC CH4. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[6]	MASK_ADC_OVERLOAD_CH3	Masks the latched ADC_OVERLOAD status bit on ADC CH3. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[5]	MASK_ADC_OVERLOAD_CH2	Masks the latched ADC_OVERLOAD status bit on ADC CH2. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[4]	MASK_ADC_OVERLOAD_CH1	Masks the latched ADC_OVERLOAD status bit on ADC CH1. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[3]	MASK_PEAK_DET_CH4	Masks the latched PEAK_FLAG status bit on ADC CH4. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[2]	MASK_PEAK_DET_CH3	Masks the latched PEAK_FLAG status bit on ADC CH3. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[1]	MASK_PEAK_DET_CH2	Masks the latched PEAK_FLAG status bit on ADC CH2. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[0]	MASK_PEAK_DET_CH1	Masks the latched PEAK_FLAG status bit on ADC CH1. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled

Register 33: STATUS BITS CLEAR

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	CLEAR_ADC_OVERLOAD_CH4	Clears the latched ADC_OVERLOAD status bit on ADC CH4. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[6]	CLEAR_ADC_OVERLOAD_CH3	Clears the latched ADC_OVERLOAD status bit on ADC CH3. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[5]	CLEAR_ADC_OVERLOAD_CH2	Clears the latched ADC_OVERLOAD status bit on ADC CH2. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[4]	CLEAR_ADC_OVERLOAD_CH1	Clears the latched ADC_OVERLOAD status bit on ADC CH1. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[3]	CLEAR_PEAK_DET_CH4	Clears the latched PEAK_FLAG status bit on ADC CH4. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[2]	CLEAR_PEAK_DET_CH3	Clears the latched PEAK_FLAG status bit on ADC CH3. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[1]	CLEAR_PEAK_DET_CH2	Clears the latched PEAK_FLAG status bit on ADC CH2. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[0]	CLEAR_PEAK_DET_CH1	Clears the latched PEAK_FLAG status bit on ADC CH1. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared

Register 46-34: RESERVED

GPIO Registers

Register 47: GPIO1/2 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO2_CFG	Configure GPIO2 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: OR of Status Bits – output • 4'd3: Clock valid flag – output • 4'd4: S/PDIF stream – output • 4'd5: PWM1 signal – output • 4'd6: PWM2 signal – output • 4'd7: PWM3 signal – output • 4'd8: Reserved • 4'd9: Reserved • 4'd10: Mute ADCs – input • 4'd11: BCK/WS Fail – output • 4'd12: CH1 Detection flag – output • 4'd13: CH2 Detection flag – output • 4'd14: CH3 Detection flag – output • 4'd15: CH4 Detection flag – output
[3:0]	GPIO1_CFG	Configure GPIO1 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: OR of Status Bits – output • 4'd3: Clock valid flag – output • 4'd4: S/PDIF stream – output • 4'd5: PWM1 signal – output • 4'd6: PWM2 signal – output • 4'd7: PWM3 signal – output • 4'd8: Reserved • 4'd9: Reserved • 4'd10: Mute ADCs – input • 4'd11: BCK/WS Fail – output • 4'd12: CH1 Detection flag – output • 4'd13: CH2 Detection flag – output • 4'd14: CH3 Detection flag – output • 4'd15: CH4 Detection flag – output

Register 48: GPIO3/4 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO4_CFG	Configure GPIO4 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: OR of Status Bits – output • 4'd3: Clock valid flag – output • 4'd4: S/PDIF stream – output • 4'd5: PWM1 signal – output • 4'd6: PWM2 signal – output • 4'd7: PWM3 signal – output • 4'd8: Reserved • 4'd9: Reserved • 4'd10: Mute ADCs – input • 4'd11: BCK/WS Fail – output • 4'd12: CH1 Detection flag – output • 4'd13: CH2 Detection flag – output • 4'd14: CH3 Detection flag – output • 4'd15: CH4 Detection flag – output
[3:0]	GPIO3_CFG	Configure GPIO3 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: OR of Status Bits – output • 4'd3: Clock valid flag – output • 4'd4: S/PDIF stream – output • 4'd5: PWM1 signal – output • 4'd6: PWM2 signal – output • 4'd7: PWM3 signal – output • 4'd8: Reserved • 4'd9: Reserved • 4'd10: Mute ADCs – input • 4'd11: BCK/WS Fail – output • 4'd12: CH1 Detection flag – output • 4'd13: CH2 Detection flag – output • 4'd14: CH3 Detection flag – output • 4'd15: CH4 Detection flag – output

Register 49: GPIO5/6 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO6_CFG	Configure GPIO6 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: OR of Status Bits – output • 4'd3: Clock valid flag – output • 4'd4: S/PDIF stream – output • 4'd5: PWM1 signal – output • 4'd6: PWM2 signal – output • 4'd7: PWM3 signal – output • 4'd8: Reserved • 4'd9: Reserved • 4'd10: Mute ADCs – input • 4'd11: BCK/WS Fail – output • 4'd12: CH1 Detection flag – output • 4'd13: CH2 Detection flag – output • 4'd14: CH3 Detection flag – output • 4'd15: CH4 Detection flag – output
[3:0]	GPIO5_CFG	Configure GPIO5 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: OR of Status Bits – output • 4'd3: Clock valid flag – output • 4'd4: S/PDIF stream – output • 4'd5: PWM1 signal – output • 4'd6: PWM2 signal – output • 4'd7: PWM3 signal – output • 4'd8: Reserved • 4'd9: Reserved • 4'd10: Mute ADCs – input • 4'd11: BCK/WS Fail – output • 4'd12: CH1 Detection flag – output • 4'd13: CH2 Detection flag – output • 4'd14: CH3 Detection flag – output • 4'd15: CH4 Detection flag – output

Register 50: GPIO7/8 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO8_CFG	Configure GPIO8 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: OR of Status Bits – output • 4'd3: Clock valid flag – output • 4'd4: S/PDIF stream – output • 4'd5: PWM1 signal – output • 4'd6: PWM2 signal – output • 4'd7: PWM3 signal – output • 4'd8: Reserved • 4'd9: Reserved • 4'd10: Mute ADCs – input • 4'd11: BCK/WS Fail – output • 4'd12: CH1 Detection flag – output • 4'd13: CH2 Detection flag – output • 4'd14: CH3 Detection flag – output • 4'd15: CH4 Detection flag – output
[3:0]	GPIO7_CFG	Configure GPIO7 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: OR of Status Bits – output • 4'd3: Clock valid flag – output • 4'd4: S/PDIF stream – output • 4'd5: PWM1 signal – output • 4'd6: PWM2 signal – output • 4'd7: PWM3 signal – output • 4'd8: Reserved • 4'd9: Reserved • 4'd10: Mute ADCs – input • 4'd11: BCK/WS Fail – output • 4'd12: CH1 Detection flag – output • 4'd13: CH2 Detection flag – output • 4'd14: CH3 Detection flag – output • 4'd15: CH4 Detection flag – output

Register 51: GPIO9/10 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO10_CFG	Configure GPIO10 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: OR of Status Bits – output • 4'd3: Clock valid flag – output • 4'd4: S/PDIF stream – output • 4'd5: PWM1 signal – output • 4'd6: PWM2 signal – output • 4'd7: PWM3 signal – output • 4'd8: Reserved • 4'd9: Reserved • 4'd10: Mute ADCs – input • 4'd11: BCK/WS Fail – output • 4'd12: CH1 Detection flag – output • 4'd13: CH2 Detection flag – output • 4'd14: CH3 Detection flag – output • 4'd15: CH4 Detection flag – output
[3:0]	GPIO9_CFG	Configure GPIO9 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: OR of Status Bits – output • 4'd3: Clock valid flag – output • 4'd4: S/PDIF stream – output • 4'd5: PWM1 signal – output • 4'd6: PWM2 signal – output • 4'd7: PWM3 signal – output • 4'd8: Reserved • 4'd9: Reserved • 4'd10: Mute ADCs – input • 4'd11: BCK/WS Fail – output • 4'd12: CH1 Detection flag – output • 4'd13: CH2 Detection flag – output • 4'd14: CH3 Detection flag – output • 4'd15: CH4 Detection flag – output

Register 52: GPIO11 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3:0]	GPIO11_CFG	Configure GPIO11 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Output 0 – output • 4'd2: OR of Status Bits – output • 4'd3: Clock valid flag – output • 4'd4: S/PDIF stream – output • 4'd5: PWM1 signal – output • 4'd6: PWM2 signal – output • 4'd7: PWM3 signal – output • 4'd8: Reserved • 4'd9: Reserved • 4'd10: Mute ADCs – input • 4'd11: BCK/WS Fail – output • 4'd12: CH1 Detection flag – output • 4'd13: CH2 Detection flag – output • 4'd14: CH3 Detection flag – output • 4'd15: CH4 Detection flag – output

Register 54-53: GPIO INPUT ENABLE

Bits	[15:11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	5'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:11]	RESERVED	N/A
[10]	GPIO11_IE	• 1'b0: GPIO11 input disabled (default) • 1'b1: GPIO11 input enabled
[9]	GPIO10_IE	• 1'b0: GPIO10 input disabled (default) • 1'b1: GPIO10 input enabled
[8]	GPIO9_IE	• 1'b0: GPIO9 input disabled (default) • 1'b1: GPIO9 input enabled
[7]	GPIO8_IE	• 1'b0: GPIO8 input disabled (default) • 1'b1: GPIO8 input enabled
[6]	GPIO7_IE	• 1'b0: GPIO7 input disabled (default) • 1'b1: GPIO7 input enabled
[5]	GPIO6_IE	• 1'b0: GPIO6 input disabled (default) • 1'b1: GPIO6 input enabled
[4]	GPIO5_IE	• 1'b0: GPIO5 input disabled (default) • 1'b1: GPIO5 input enabled
[3]	GPIO4_IE	• 1'b0: GPIO4 input disabled (default) • 1'b1: GPIO4 input enabled
[2]	GPIO3_IE	• 1'b0: GPIO3 input disabled (default) • 1'b1: GPIO3 input enabled
[1]	GPIO2_IE	• 1'b0: GPIO2 input disabled (default) • 1'b1: GPIO2 input enabled
[0]	GPIO1_IE	• 1'b0: GPIO1 input disabled (default) • 1'b1: GPIO1 input enabled

Register 56-55: GPIO OUTPUT ENABLE

Bits	[15:11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	5'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:11]	RESERVED	N/A
[10]	GPIO11_OE	• 1'b0: Tristate GPIO11 output (default) • 1'b1: GPIO11 output enabled
[9]	GPIO10_OE	• 1'b0: Tristate GPIO10 output (default) • 1'b1: GPIO10 output enabled
[8]	GPIO9_OE	• 1'b0: Tristate GPIO9 output (default) • 1'b1: GPIO9 output enabled
[7]	GPIO8_OE	• 1'b0: Tristate GPIO8 output (default) • 1'b1: GPIO8 output enabled
[6]	GPIO7_OE	• 1'b0: Tristate GPIO7 output (default) • 1'b1: GPIO7 output enabled
[5]	GPIO6_OE	• 1'b0: Tristate GPIO6 output (default) • 1'b1: GPIO6 output enabled
[4]	GPIO5_OE	• 1'b0: Tristate GPIO5 output (default) • 1'b1: GPIO5 output enabled
[3]	GPIO4_OE	• 1'b0: Tristate GPIO4 output (default) • 1'b1: GPIO4 output enabled
[2]	GPIO3_OE	• 1'b0: Tristate GPIO3 output (default) • 1'b1: GPIO3 output enabled
[1]	GPIO2_OE	• 1'b0: Tristate GPIO2 output (default) • 1'b1: GPIO2 output enabled
[0]	GPIO1_OE	• 1'b0: Tristate GPIO1 output (default) • 1'b1: GPIO1 output enabled

Register 58-57: GPIO INVERT

Bits	[15:11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	5'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:11]	RESERVED	N/A
[10]	GPIO11_INV	Invert the GPIO11 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[9]	GPIO10_INV	Invert the GPIO10 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[8]	GPIO9_INV	Invert the GPIO9 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[7]	GPIO8_INV	Invert the GPIO8 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[6]	GPIO7_INV	Invert the GPIO7 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[5]	GPIO6_INV	Invert the GPIO6 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[4]	GPIO5_INV	Invert the GPIO5 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[3]	GPIO4_INV	Invert the GPIO4 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[2]	GPIO3_INV	Invert the GPIO3 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[1]	GPIO2_INV	Invert the GPIO2 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	GPIO1_INV	Invert the GPIO1 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted

Register 60-59: GPIO WEAK KEEPER

Bits	[15:11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	5'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:11]	RESERVED	N/A
[10]	GPIO11_WK_EN	• 1'b0: GPIO11 weak keeper disabled (default) • 1'b1: GPIO11 weak keeper enabled
[9]	GPIO10_WK_EN	• 1'b0: GPIO10 weak keeper disabled (default) • 1'b1: GPIO10 weak keeper enabled
[8]	GPIO9_WK_EN	• 1'b0: GPIO9 weak keeper disabled (default) • 1'b1: GPIO9 weak keeper enabled
[7]	GPIO8_WK_EN	• 1'b0: GPIO8 weak keeper disabled (default) • 1'b1: GPIO8 weak keeper enabled
[6]	GPIO7_WK_EN	• 1'b0: GPIO7 weak keeper disabled (default) • 1'b1: GPIO7 weak keeper enabled
[5]	GPIO6_WK_EN	• 1'b0: GPIO6 weak keeper disabled (default) • 1'b1: GPIO6 weak keeper enabled
[4]	GPIO5_WK_EN	• 1'b0: GPIO5 weak keeper disabled (default) • 1'b1: GPIO5 weak keeper enabled
[3]	GPIO4_WK_EN	• 1'b0: GPIO4 weak keeper disabled (default) • 1'b1: GPIO4 weak keeper enabled
[2]	GPIO3_WK_EN	• 1'b0: GPIO3 weak keeper disabled (default) • 1'b1: GPIO3 weak keeper enabled
[1]	GPIO2_WK_EN	• 1'b0: GPIO2 weak keeper disabled (default) • 1'b1: GPIO2 weak keeper enabled
[0]	GPIO1_WK_EN	• 1'b0: GPIO1 weak keeper disabled (default) • 1'b1: GPIO1 weak keeper enabled

Register 62-61: GPIO READ

Bits	[15:11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	5'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:11]	RESERVED	N/A
[10]	GPIO11_READ	• 1'b0: GPIO11 input readback disabled (default) • 1'b1: Allows readback of GPIO11 input
[9]	GPIO10_READ	• 1'b0: GPIO10 input readback disabled (default) • 1'b1: Allows readback of GPIO10 input
[8]	GPIO9_READ	• 1'b0: GPIO9 input readback disabled (default) • 1'b1: Allows readback of GPIO9 input
[7]	GPIO8_READ	• 1'b0: GPIO8 input readback disabled (default) • 1'b1: Allows readback of GPIO8 input
[6]	GPIO7_READ	• 1'b0: GPIO7 input readback disabled (default) • 1'b1: Allows readback of GPIO7 input
[5]	GPIO6_READ	• 1'b0: GPIO6 input readback disabled (default) • 1'b1: Allows readback of GPIO6 input
[4]	GPIO5_READ	• 1'b0: GPIO5 input readback disabled (default) • 1'b1: Allows readback of GPIO5 input
[3]	GPIO4_READ	• 1'b0: GPIO4 input readback disabled (default) • 1'b1: Allows readback of GPIO4 input
[2]	GPIO3_READ	• 1'b0: GPIO3 input readback disabled (default) • 1'b1: Allows readback of GPIO3 input
[1]	GPIO2_READ	• 1'b0: GPIO2 input readback disabled (default) • 1'b1: Allows readback of GPIO2 input
[0]	GPIO1_READ	• 1'b0: GPIO1 input readback disabled (default) • 1'b1: Allows readback of GPIO1 input

Register 63: DETECTION FLAG CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	LIVE_DETECT_CH4	Set the CH4 detection flag to use the live value, instead of the latched value. • 1'b0: Latched flag (default) • 1'b1: Live flag
[6]	LIVE_DETECT_CH3	Set the CH3 detection flag to use the live value, instead of the latched value. • 1'b0: Latched flag (default) • 1'b1: Live flag
[5]	LIVE_DETECT_CH2	Set the CH2 detection flag to use the live value, instead of the latched value. • 1'b0: Latched flag (default) • 1'b1: Live flag
[4]	LIVE_DETECT_CH1	Set the CH1 detection flag to use the live value, instead of the latched value. • 1'b0: Latched flag (default) • 1'b1: Live flag
[3]	DETECT_FLAG_SEL_CH4	Selects which CH4 detection flag to output when gpio_cfg is set to "CH4 Detection Flag". • 1'b0: Peak Detect Flag (default) • 1'b1: ADC Overload Flag
[2]	DETECT_FLAG_SEL_CH3	Selects which CH3 detection flag to output when gpio_cfg is set to "CH3 Detection Flag". • 1'b0: Peak Detect Flag (default) • 1'b1: ADC Overload Flag
[1]	DETECT_FLAG_SEL_CH2	Selects which CH2 detection flag to output when gpio_cfg is set to "CH2 Detection Flag". • 1'b0: Peak Detect Flag (default) • 1'b1: ADC Overload Flag
[0]	DETECT_FLAG_SEL_CH1	Selects which CH1 detection flag to output when gpio_cfg is set to "CH1 Detection Flag". • 1'b0: Peak Detect Flag (default) • 1'b1: ADC Overload Flag

Register 64: PWM1 COUNT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	PWM1_COUNT	8-bit value for the number of MCLK periods the PWM signal is high. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 66-65: PWM1 FREQUENCY

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	PWM1_FREQ	16-bit value for the frequency of the PWM signal. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $\text{Frequency [Hz]} = \frac{\text{MCLK}}{\text{PWM1\_FREQ} + 1}$ $\text{Duty Cycle [\%]} = \frac{\text{PWM1\_COUNT}}{\text{PWM1\_FREQ} + 1} \cdot 100$

Register 67: PWM2 COUNT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	PWM2_COUNT	8-bit value for the number of MCLK periods the PWM signal is high. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 69-68: PWM2 FREQUENCY

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	PWM2_FREQ	16-bit value for the frequency of the PWM signal. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $\text{Frequency [Hz]} = \frac{\text{MCLK}}{\text{PWM2\_FREQ} + 1}$ $\text{Duty Cycle [\%]} = \frac{\text{PWM2\_COUNT}}{\text{PWM2\_FREQ} + 1} \cdot 100$

Register 70: PWM3 COUNT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	PWM3_COUNT	8-bit value for the number of MCLK periods the PWM signal is high. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 72-71: PWM3 FREQUENCY

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	PWM3_FREQ	16-bit value for the frequency of the PWM signal. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $\text{Frequency [Hz]} = \frac{\text{MCLK}}{\text{PWM3\_FREQ} + 1}$ $\text{Duty Cycle [\%]} = \frac{\text{PWM3\_COUNT}}{\text{PWM3\_FREQ} + 1} \cdot 100$

ADC Registers

Register 73: ADC NEGATION

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	4'b0000	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	ADC_NEG_SEL_CH4	Inverts data input from the CH4 analog ADC. • 1'b0: No inversion (default) • 1'b1: Inverts input data
[2]	ADC_NEG_SEL_CH3	Inverts data input from the CH3 analog ADC. • 1'b0: No inversion (default) • 1'b1: Inverts input data
[1]	ADC_NEG_SEL_CH2	Inverts data input from the CH2 analog ADC. • 1'b0: No inversion (default) • 1'b1: Inverts input data
[0]	ADC_NEG_SEL_CH1	Inverts data input from the CH1 analog ADC. • 1'b0: No inversion (default) • 1'b1: Inverts input data

Register 74: ADC FIR FILTER

Bits	[7:5]	[4]	[3]	[2:0]
Default	3'd0	1'b0	1'b0	3'b000

Bits	Mnemonic	Description
[7:5]	FILTER_SHAPE	Selects the 8x decimation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase fast roll-off apodizing • 3'd2: Linear phase fast roll-off • 3'd3: Linear phase fast roll-off low ripple • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion
[4]	BYPASS_FIR2X	• 1'b0: Non-bypass (default) • 1'b1: Bypass DFir_2x
[3]	BYPASS_FIR4X	• 1'b0: Non-bypass (default) • 1'b1: Bypass DFir_4x
[2:0]	BYPASS_IIR	Bypass IIR Filter. • 3'b000: Non-bypass (default) • 3'b111: Bypass IIR • Others: Reserved

Register 75: RESERVED

Register 76: DC BLOCKING

Bits	[7]	[6]	[5]	[4]	[3:0]
Default	1'b1	1'b1	1'b1	1'b1	4'b0010

Bits	Mnemonic	Description
[7]	DC_BLOCK_EN_CH4	Enable the CH4 DC blocking filter on audio datapath. • 1'b0: Bypass DC blocking filter • 1'b1: Use DC blocking filter (default)
[6]	DC_BLOCK_EN_CH3	Enable the CH3 DC blocking filter on audio datapath. • 1'b0: Bypass DC blocking filter • 1'b1: Use DC blocking filter (default)
[5]	DC_BLOCK_EN_CH2	Enable the CH2 DC blocking filter on audio datapath. • 1'b0: Bypass DC blocking filter • 1'b1: Use DC blocking filter (default)
[4]	DC_BLOCK_EN_CH1	Enable the CH1 DC blocking filter on audio datapath. • 1'b0: Bypass DC blocking filter • 1'b1: Use DC blocking filter (default)
[3:0]	RESERVED	N/A

Register 80-77: RESERVED

Register 81: VOLUME CH1

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	VOLUME_CH1	CH1 volume. 0dB to -127dB, 0.5dB steps. • 8'h00: 0dB (default) • 8'hFE: -127dB • 8'hFF: Mute

Register 82: VOLUME CH2

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	VOLUME_CH2	CH2 volume. 0dB to -127dB, 0.5dB steps. • 8'h00: 0dB (default) • 8'hFE: -127dB • 8'hFF: Mute

Register 83: VOLUME CH3

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	VOLUME_CH3	CH3 volume. 0dB to -127dB, 0.5dB steps. • 8'h00: 0dB (default) • 8'hFE: -127dB • 8'hFF: Mute

Register 84: VOLUME CH4

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	VOLUME_CH4	CH4 volume. 0dB to -127dB, 0.5dB steps. • 8'h00: 0dB (default) • 8'hFE: -127dB • 8'hFF: Mute

Register 86-85: DIGITAL GAIN

Bits	[15]	[14:12]	[11]	[10:8]	[7]	[6:4]	[3]	[2:0]
Default	1'b0	3'd0	1'b0	3'd0	1'b0	3'd0	1'b0	3'd0

Bits	Mnemonic	Description
[15]	MONO_VOLUME	All channel volumes controlled by the CH1 volume control. • 1'b0: Disabled (default) • 1'b1: Enabled
[14:12]	DIGITAL_GAIN_CH4	ADC CH4 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'dn: +(n*6)dB
[11]	RESERVED	N/A
[10:8]	DIGITAL_GAIN_CH3	ADC CH3 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'dn: +(n*6)dB
[7]	RESERVED	N/A
[6:4]	DIGITAL_GAIN_CH2	ADC CH2 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'dn: +(n*6)dB
[3]	RESERVED	N/A
[2:0]	DIGITAL_GAIN_CH1	ADC CH1 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'dn: +(n*6)dB

Register 87: PHASE INVERSION

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	4'd0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	VOL_PHASE_INV_CH4	Inverts the phase of VOLUME_CH4. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[2]	VOL_PHASE_INV_CH3	Inverts the phase of VOLUME_CH3. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[1]	VOL_PHASE_INV_CH2	Inverts the phase of VOLUME_CH2. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	VOL_PHASE_INV_CH1	Inverts the phase of VOLUME_CH1. • 1'b0: Non-inverted (default) • 1'b1: Inverted

Register 88: VOLUME UP RAMP RATE

Bits	[7:0]
Default	8'h04

Bits	Mnemonic	Description
[7:0]	VOL_RAMP_RATE_UP	Linear step size from current volume to target volume, represented as a fraction of full-scale. $\text{ramp\_step [inc/sample]} = \frac{\text{VOL\_RAMP\_RATE\_UP}}{2^{12}}$ • 8'h00: Instant change • 8'h01: Slowest change • 8'h04: Default • 8'hFF: Fastest change

Register 89: VOLUME DOWN RAMP RATE

Bits	[7:0]
Default	8'h04

Bits	Mnemonic	Description
[7:0]	VOL_RAMP_RATE_DOWN	Linear step size from current volume to target volume, represented as a fraction of full-scale. $\text{ramp\_step [dec/sample]} = \frac{\text{VOL\_RAMP\_RATE\_DOWN}}{2^{12}}$ • 8'h00: Instant change • 8'h01: Slowest change • 8'h04: Default • 8'hFF: Fastest change

Register 91-90: THD COMP C2 CH1/2

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	THD_COMP_C2_CH12	A 16-bit signed coefficient for correcting for the ADC 2nd harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$

Register 93-92: THD COMP C3 CH1/2

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	THD_COMP_C3_CH12	A 16-bit signed coefficient for correcting the ADC 3rd harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$ Note: Register value is XOR'd with 16'hFFD8

Register 95-94: THD COMP C2 CH3/4

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	THD_COMP_C2_CH34	A 16-bit signed coefficient for correcting for the ADC 2nd harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$

Register 97-96: THD COMP C3 CH3/4

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	THD_COMP_C3_CH34	A 16-bit signed coefficient for correcting for the ADC 3rd harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$ Note: Register value is XOR'd with 16'hFFD8

Register 98: PEAK DETECT ENABLE

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	4'd0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	PEAK_DETECT_EN_CH4	Enables the ADC CH4 peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	PEAK_DETECT_EN_CH3	Enables the ADC CH3 peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	PEAK_DETECT_EN_CH2	Enables the ADC CH2 peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	PEAK_DETECT_EN_CH1	Enables the ADC CH1 peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 99: PEAK DETECT CONFIG

Bits	[7]	[6]	[5]	[4:0]
Default	1'd0	1'b0	1'b0	5'd10

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	LOCK_PEAK_VALUE	Locks the current peak detector values, for reading back. • 1'b0: Peak detector value can update (default) • 1'b1: Peak detector value locked
[5]	RESERVED	N/A
[4:0]	PEAK_DECAY_RATE	Sets the speed at which the peak detector value will decay when greater than the input signal. • 5'd0: Instant decay • 5'd1: Fastest decay • 5'd10: Default value • 5'd22: Slowest decay • Others: Reserved

Register 103-100: PEAK THRESHOLDS

Bits	[31:24]	[23:16]	[15:8]	[7:0]
Default	8'hFF	8'hFF	8'hFF	8'hFF

Bits	Mnemonic	Description
[31:24]	PEAK_THRESH_CH4	Threshold value to trigger the PEAK_FLAG in the CH4 peak detector. Triggers if the input signal > PEAK_THRESH_CH4. • 8'h01: -48dB • 8'hFF: 0dB (default) $\text{threshold [dB]} = 20 \cdot \log10\left(\left(\frac{\text{PEAK\_THRESH\_CH4}}{2^8 - 1}\right) \cdot \left(\frac{32}{30}\right)\right)$
[23:16]	PEAK_THRESH_CH3	Threshold value to trigger the PEAK_FLAG in the CH3 peak detector. Triggers if the input signal > PEAK_THRESH_CH3. • 8'h01: -48dB • 8'hFF: 0dB (default) $\text{threshold [dB]} = 20 \cdot \log10\left(\left(\frac{\text{PEAK\_THRESH\_CH3}}{2^8 - 1}\right) \cdot \left(\frac{32}{30}\right)\right)$
[15:8]	PEAK_THRESH_CH2	Threshold value to trigger the PEAK_FLAG in the CH2 peak detector. Triggers if the input signal > PEAK_THRESH_CH2. • 8'h01: -48dB • 8'hFF: 0dB (default) $\text{threshold [dB]} = 20 \cdot \log10\left(\left(\frac{\text{PEAK\_THRESH\_CH2}}{2^8 - 1}\right) \cdot \left(\frac{32}{30}\right)\right)$
[7:0]	PEAK_THRESH_CH1	Threshold value to trigger the PEAK_FLAG in the CH1 peak detector. Triggers if the input signal > PEAK_THRESH_CH1. • 8'h01: -48dB • 8'hFF: 0dB (default) $\text{threshold [dB]} = 20 \cdot \log10\left(\left(\frac{\text{PEAK\_THRESH\_CH1}}{2^8 - 1}\right) \cdot \left(\frac{32}{30}\right)\right)$

Register 106-104: RESERVED

PLL Registers

Register 107: PLL CLOCK SELECT

Bits	[7]	[6]	[5:4]	[3]	[2]	[1:0]
Default	1'b0	1'b0	2'b10	1'b0	1'b0	2'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	PLL_CLK_PHASE_INV	Digital/analog DAC clock invert phase enable. • 1'b0: Digital/analog DAC clocks have inverted phase (default) • 1'b1: Digital/analog DAC clocks have the same phase
[5:4]	SEL_PLL_CLK_IN	Selects PLL input clock source when EN_PLL_CLK_IN is set. • 2'b00: ACLK1 • 2'b01: ACLK2 • 2'b10: DATA_CLK (default)
[3]	EN_PLL_CLK_IN	Allows SEL_PLL_CLK_IN to select PLL input clocks. • 1'b0: Disables SEL_PLL_CLK_IN (default) • 1'b1: Enables SEL_PLL_CLK_IN
[2]	SEL_MCLK_IN_PLL	Selects which ACLK source is used by the digital core and analog ADC, when EN_MCLK_IN is set. • 1'b0: ACLK1/2 (default) • 1'b1: PLL_CLK Note: Overrides SEL_MCLK_ACLK_SRC.
[1:0]	RESERVED	N/A

Register 108: PLL VCO & CP

Bits	[7]	[6:4]	[3]	[2]	[1]	[0]
Default	1'b0	3'b011	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:4]	PLL_CP_BIAS_SEL	Sets the PLL Charge Pump bias Current: • 3'b001: (recommended for ASYNC PLL case) • 3'b011: (default)
[3]	PLL_CP_EN	Enable the PLL charge pump. • 1'b0: PLL Charge Pump Disabled (default) • 1'b1: PLL Charge Pump Enabled
[2]	PLL_VCO_EN	Enable the PLL voltage-controlled oscillator (VCO). • 1'b0: PLL VCO Disabled (default) • 1'b1: PLL VCO Enabled
[1]	PLL_CLKSMP_EN	Enable the PLL circuitry. • 1'b0: PLL Block Disabled (default) • 1'b1: PLL Block Enabled
[0]	PLL_DIG_RSTB	Enable the Digital block of the PLL. • 1'b0: PLL Digital block disabled (default) • 1'b1: PLL Digital block enabled

Register 109: PLL REGULATOR

Bits	[7:4]	[3]	[2]	[1:0]
Default	4'd0	1'b0	1'b0	2'b10

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	PLL_REG_EN	Enable the PLL regulator. • 1'b0: PLL Regulator Disabled (default) • 1'b1: PLL Regulator Enabled
[2]	PLL_REG_LN	Enable Low Noise Reference for PLL regulator. • 1'b0: PLL Low Noise Reference Disabled (default) • 1'b1: PLL Low Noise Reference Enabled
[1:0]	RESERVED	N/A

Register 112-110: PLL FEEDBACK DIV

Bits	[23:0]
Default	24'h100000

Bits	Mnemonic	Description
[23:0]	PLL_CLK_FB_DIV	Sets the PLL clock feedback divider (Nfb). • 24'h000000: Reserved • 24'h100000: Default • 24'hn: Divide by 2^25/n

Register 115-113: PLL IN & OUT DIV

Bits	[23:21]	[20]	[19:16]	[15:12]	[11:10]	[9]	[8:0]
Default	3'd0	1'b1	4'd0	4'd3	2'd0	1'b1	9'd0

Bits	Mnemonic	Description
[23:21]	RESERVED	N/A
[20]	PLL_CLK_OUT_DIV_PHASE_EN	Sets the tuning mode for the PLL_CLK_OUT_DIV phase. • 1'b0: Dynamic Tuning of Phase • 1'b1: Static Tuning of Phase (default)
[19:16]	RESERVED	N/A
[15:12]	PLL_CLK_OUT_DIV	Sets the PLL clock output divider (No). • 4'd0: Reserved • 4'd3: Divide by 4. (default) • 4'dn: Divide by (n + 1).
[11:10]	RESERVED	N/A
[9]	PLL_FB_DIV_LOAD	Write 1'b1 then write 1'b0 to load CLK_FB_DIV.
[8:0]	PLL_CLK_IN_DIV	Sets the PLL clock input divider (Ni). • 9'd0: Reserved (default) • 9'dn: Divide by (n + 1).

Register 116: PLL VCO CONTROL 1

Bits	[7:2]	[1:0]
Default	6'b010000	2'b00

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1:0]	VCO_IB_AMP_CTRL	Selects the VCO bias current: • 2'b00 (default) • 2'b10 (recommended for ASYNC PLL case)

Register 121-117: RESERVED

SPI Master Registers

Register 122: SPI MASTER CONFIG

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	4'd0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:4]	SPI_M_PULSE_WIDTH	Sets the master SCLK frequency. $\text{SCLK [Hz]} = \frac{\text{MCLK}}{2 \cdot \text{SPI\_M\_PULSE\_WIDTH}}$
[3]	SPI_M_EN	Enable the SPI Master • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	SPI_M_MODE	SPI Mode • 1'b0: Mode 0 (default) • 1'b1: Mode 3
[1]	SPI_M_SEND_BYTE	Triggers the SPI master to send the current byte in SPI_M_DATA_O to the slave device. • 1'b0: Do not send byte (default) • 1'b1: Send byte to SPI slave device
[0]	SPI_M_START	Start/stop SPI master transactions. • 1'b0: Transactions stopped (default) • 1'b1: Transactions started

Register 123: SPI MASTER DATA OUT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	SPI_M_DATA_O	Data byte to send over the SPI master interface.

Readback Registers

Register 224: VALIDITY READ

Bits	[7]	[6]	[5]	[4:0]
Default	-	-	-	-

Bits	Mnemonic	Description
[7]	PLL_LOCKED	PLL locked flag.
[6]	RESERVED	N/A
[5]	TDM_ENC_VALID	TDM encoder valid flag.
[4:0]	AUTO_CH_NUM	Automatic TDM channel number tuning result.

Register 225: CHIP ID

Bits	[7:0]
Default	8'h91

Bits	Mnemonic	Description
[7:0]	CHIP_ID	• ES9841: 0x91

Register 229-226: RESERVED

Register 230: AUTO FS READ

Bits	[7]	[6]	[5:0]
Default	-	-	-

Bits	Mnemonic	Description
[7]	EN_64FS_MODE_AUTO	Result {Z} of the automatic sample rate detect (reg0[3] AUTO_FS_DETECT) logic, running the device in 64FS mode. • 1'b0: 64FS disabled • 1'b1: 64FS enabled
[6]	MCLK_128FS_HALF_DIV_AUTO	Result {Y} of the automatic sample rate detect (reg0[3] AUTO_FS_DETECT) logic. • 1'b0: MCLK_128FS is an integer multiple of MCLK, Y = 1. • 1'b1: MCLK_128FS is a (X+1)*0.5 multiple of MCLK, Y = 2.
[5:0]	MCLK_128FS_DIV_AUTO	Result {X} of the automatic sample rate detect (reg0[3] AUTO_FS_DETECT) logic. $\text{FS [Hz]} = \frac{Y \cdot \text{MCLK}}{(X+1) \cdot \left(\frac{128}{2^Z}\right)}$

Register 231: CLOCK VALIDITY

Bits	[7:3]	[2]	[1]	[0]
Default	-	-	-	-

Bits	Mnemonic	Description
[7:3]	RESERVED	N/A
[2]	RATIO_VALID	Validity of the MCLK/MCLK_128FS ratio. • 1'b0: Invalid ratio • 1'b1: Valid ratio
[1]	BCK_INVALID	Validity of the BCK signal, requires BCK_MONITOR to be enabled.
[0]	WS_INVALID	Validity of the WS signal, requires WS_MONITOR to be enabled.

Register 233-232: GPIO READBACK

Bits	[15:11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[15:11]	RESERVED	N/A
[10]	GPIO11_R	GPIO11 input readback.
[9]	GPIO10_R	GPIO10 input readback.
[8]	GPIO9_R	GPIO9 input readback.
[7]	GPIO8_R	GPIO8 input readback.
[6]	GPIO7_R	GPIO7 input readback.
[5]	GPIO6_R	GPIO6 input readback.
[4]	GPIO5_R	GPIO5 input readback.
[3]	GPIO4_R	GPIO4 input readback.
[2]	GPIO3_R	GPIO3 input readback.
[1]	GPIO2_R	GPIO2 input readback.
[0]	GPIO1_R	GPIO1 input readback.

Register 234: ADC OVERLOAD FLAGS

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	ADC_OVERLOAD_FLAG_CH4	CH4 ADC modulator overload flag. • 1'b0: No overload • 1'b1: ADC modulator overloaded
[6]	ADC_OVERLOAD_FLAG_CH3	CH3 ADC modulator overload flag. • 1'b0: No overload • 1'b1: ADC modulator overloaded
[5]	ADC_OVERLOAD_FLAG_CH2	CH2 ADC modulator overload flag. • 1'b0: No overload • 1'b1: ADC modulator overloaded
[4]	ADC_OVERLOAD_FLAG_CH1	CH1 ADC modulator overload flag. • 1'b0: No overload • 1'b1: ADC modulator overloaded
[3]	ADC_OVERLOAD_FLAG_LAT_CH4	Latched CH4 ADC modulator overload flag. • 1'b0: No overload • 1'b1: ADC modulator overloaded Note: Requires Reg 33[7] to clear flag.
[2]	ADC_OVERLOAD_FLAG_LAT_CH3	Latched CH3 ADC modulator overload flag. • 1'b0: No overload • 1'b1: ADC modulator overloaded Note: Requires Reg 33[6] to clear flag.
[1]	ADC_OVERLOAD_FLAG_LAT_CH2	Latched CH2 ADC modulator overload flag. • 1'b0: No overload • 1'b1: ADC modulator overloaded Note: Requires Reg 33[5] to clear flag.
[0]	ADC_OVERLOAD_FLAG_LAT_CH1	Latched CH1 ADC modulator overload flag. • 1'b0: No overload • 1'b1: ADC modulator overloaded Note: Requires Reg 33[4] to clear flag.

Register 235: PEAK FLAGS

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	PEAK_FLAG_CH4	ADC CH4 live peak detector flag. • 1'b0: CH4 input signal ≤ PEAK_THRESH_CH4 • 1'b1: CH4 input signal > PEAK_THRESH_CH4
[6]	PEAK_FLAG_CH3	ADC CH3 live peak detector flag. • 1'b0: CH3 input signal ≤ PEAK_THRESH_CH3 • 1'b1: CH3 input signal > PEAK_THRESH_CH3
[5]	PEAK_FLAG_CH2	ADC CH2 live peak detector flag. • 1'b0: CH2 input signal ≤ PEAK_THRESH_CH2 • 1'b1: CH2 input signal > PEAK_THRESH_CH2
[4]	PEAK_FLAG_CH1	ADC CH1 live peak detector flag. • 1'b0: CH1 input signal ≤ PEAK_THRESH_CH1 • 1'b1: CH1 input signal > PEAK_THRESH_CH1
[3]	PEAK_FLAG_LAT_CH4	ADC CH4 latched peak detector flag. • 1'b0: CH4 input signal ≤ PEAK_THRESH_CH4 • 1'b1: CH4 input signal > PEAK_THRESH_CH4 Note: Requires Reg33[3] to clear flag.
[2]	PEAK_FLAG_LAT_CH3	ADC CH3 latched peak detector flag. • 1'b0: CH3 input signal ≤ PEAK_THRESH_CH3 • 1'b1: CH3 input signal > PEAK_THRESH_CH3 Note: Requires Reg33[2] to clear flag.
[1]	PEAK_FLAG_LAT_CH2	ADC CH2 latched peak detector flag. • 1'b0: CH2 input signal ≤ PEAK_THRESH_CH2 • 1'b1: CH2 input signal > PEAK_THRESH_CH2 Note: Requires Reg33[1] to clear flag.
[0]	PEAK_FLAG_LAT_CH1	ADC CH1 latched peak detector flag. • 1'b0: CH1 input signal ≤ PEAK_THRESH_CH1 • 1'b1: CH1 input signal > PEAK_THRESH_CH1 Note: Requires Reg33[0] to clear flag.

Register 237-236: PEAK CH1 READ

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	PEAK_LEVEL_CH1	ADC CH1 peak detector value readback. $\text{Peak [dB]} = 20 \cdot \log10\left(\left(\frac{\text{PEAK\_LEVEL\_CH1}}{2^{16}-1}\right) \cdot \left(\frac{32}{30}\right)\right)$

Register 239-238: PEAK CH2 READ

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	PEAK_LEVEL_CH2	ADC CH2 peak detector value readback. $\text{Peak [dB]} = 20 \cdot \log10\left(\left(\frac{\text{PEAK\_LEVEL\_CH2}}{2^{16}-1}\right) \cdot \left(\frac{32}{30}\right)\right)$

Register 241-240: PEAK CH3 READ

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	PEAK_LEVEL_CH3	ADC CH3 peak detector value readback. $\text{Peak [dB]} = 20 \cdot \log10\left(\left(\frac{\text{PEAK\_LEVEL\_CH3}}{2^{16}-1}\right) \cdot \left(\frac{32}{30}\right)\right)$

Register 243-242: PEAK CH4 READ

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	PEAK_LEVEL_CH4	ADC CH4 peak detector value readback. $\text{Peak [dB]} = 20 \cdot \log10\left(\left(\frac{\text{PEAK\_LEVEL\_CH4}}{2^{16}-1}\right) \cdot \left(\frac{32}{30}\right)\right)$

Register 246-244: RESERVED

Register 247: SPI MASTER DATA IN

Bits	[7:0]
Default	-

Bits	Mnemonic	Description
[7:0]	SPI_M_DATA_I	Byte of data read from the SPI slave device.

ES9841Q Reference Schematic

Hardware (HW) Mode

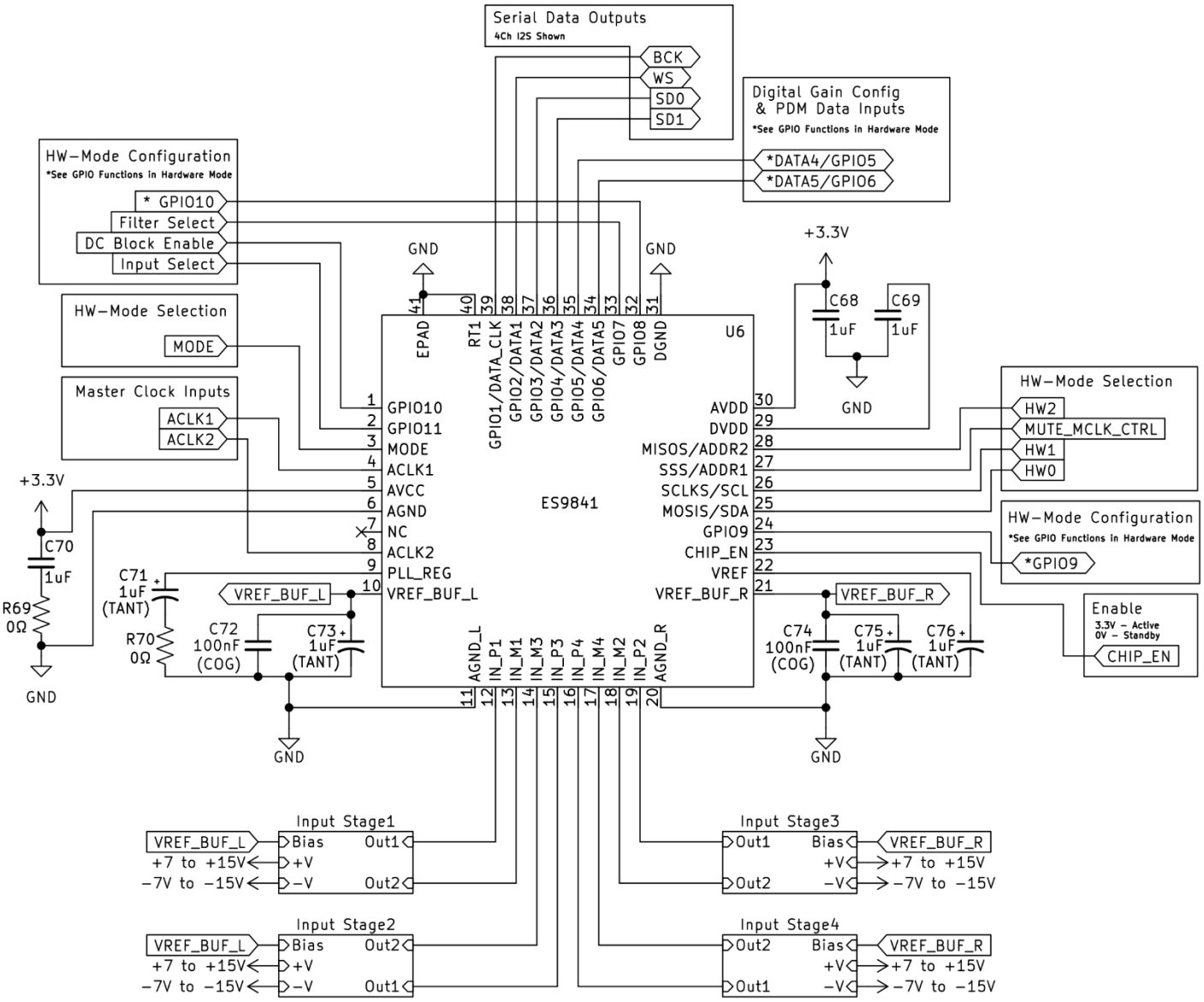


Figure 26 - ES9841Q Hardware Mode Reference Schematic

Note: The ES9841Q 40QFN package has an exposed pad (Pin 41) that should be connected to ground.

Note: It is recommended to use decoupling capacitors with the lowest ESR (Equivalent Series Resistance) available.

Note: It is recommended to use Tantalum and COG capacitors (where indicated) to achieve the highest performance.

Software (SW) Mode

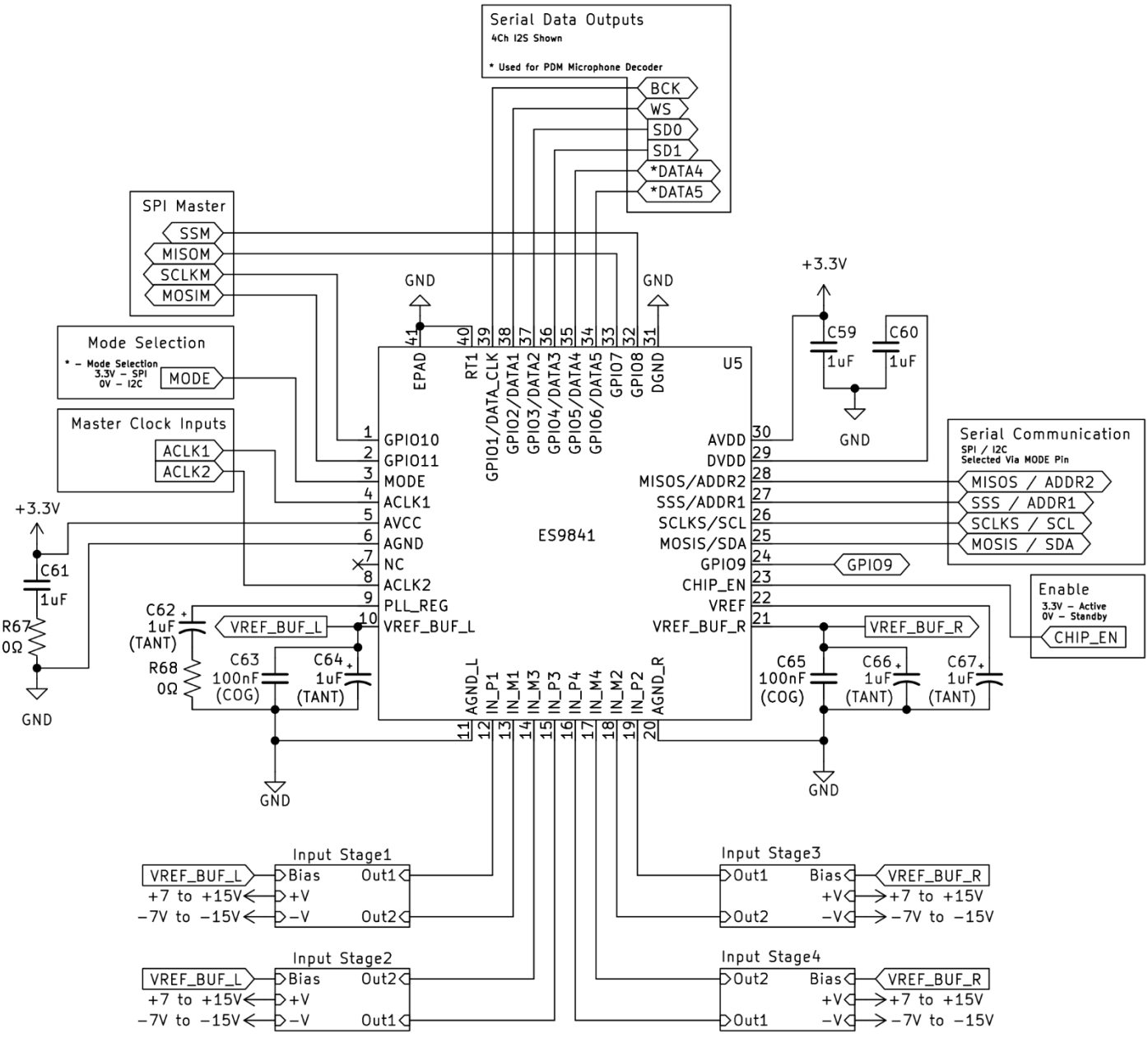


Figure 27 - ES9841Q Software Mode Reference Schematic

Note: The ES9841Q 40QFN package has an exposed pad (Pin 41) that should be connected to ground.

Note: It is recommended to use decoupling capacitors with the lowest ESR (Equivalent Series Resistance) available.

Note: It is recommended to use Tantalum and COG capacitors (where indicated) to achieve the highest performance

Differential Input Stage

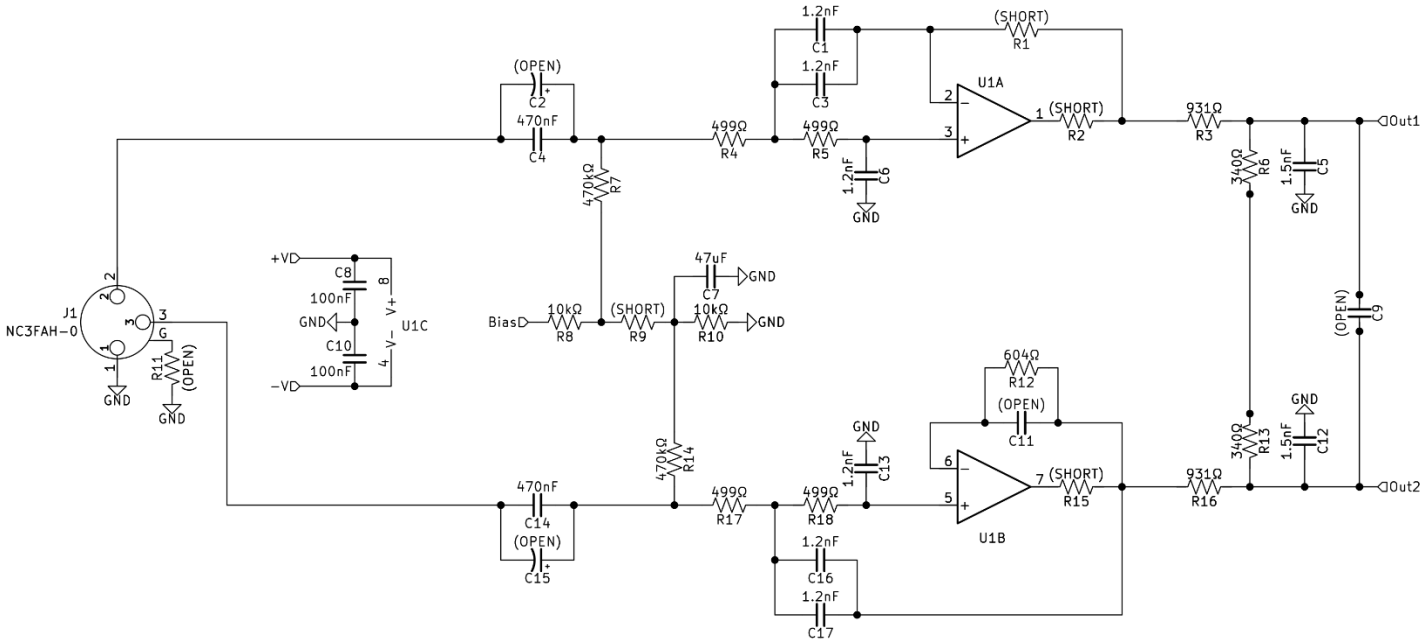


Figure 28 - Recommended Differential Input Stage

Single-Ended Input Stage

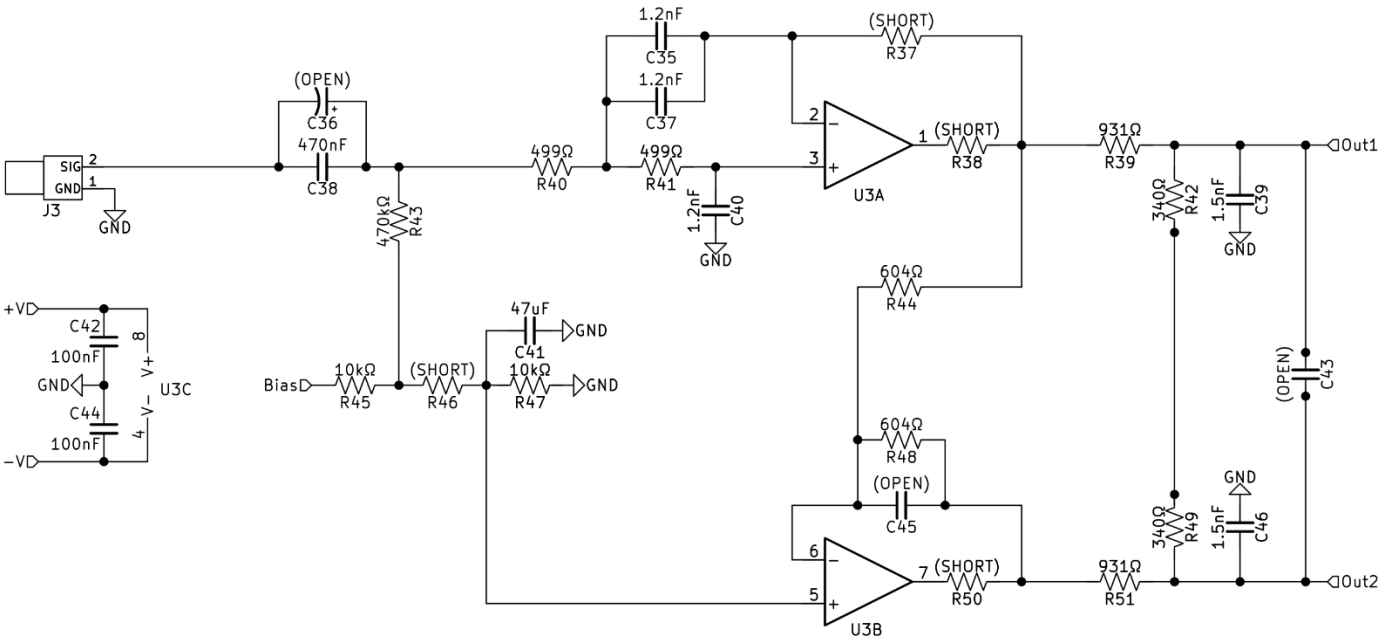


Figure 29 - Recommended Single-Ended Input Stage

ES9841 PCB Layout Guidelines

To maximize performance of the ES9841, ESS Technology makes the following PCB Layout recommendations:

1. Use of a 4+ layer PCB with an uninterrupted ground plane immediately beneath the chip. Both analog and digital ground signal can be connected here.
2. All bypass capacitors to be placed as close to the chip as possible while keeping clear ground paths between them and the chip's ground pins.
3. The use of multiple vias for each supply near its bypass capacitor and chip ground pin.
4. Minimize the use of vias for high-speed data and clock lines and avoid routing them near or directly underneath the analog output signals.
5. Ensure the package pad is connected to ground plane on the back side of the PCB with multiple vias for heat dissipation.

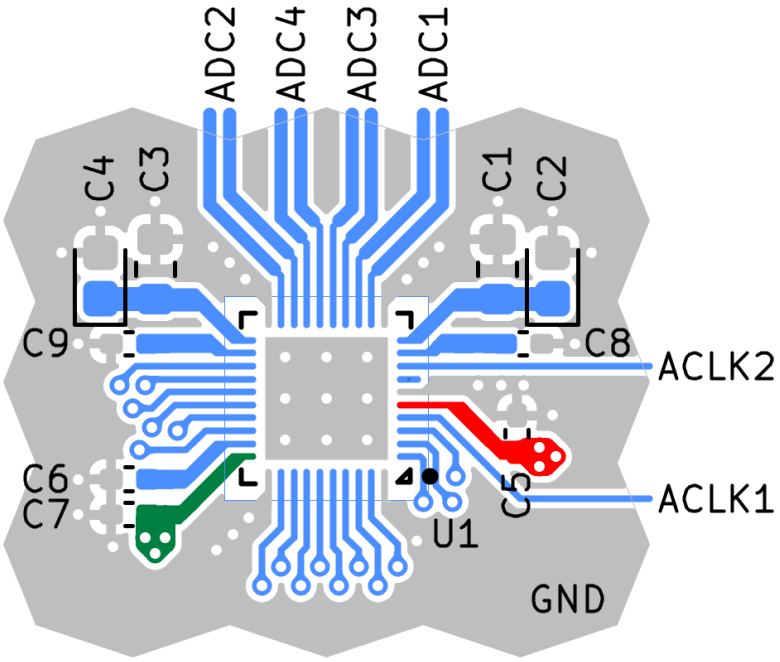
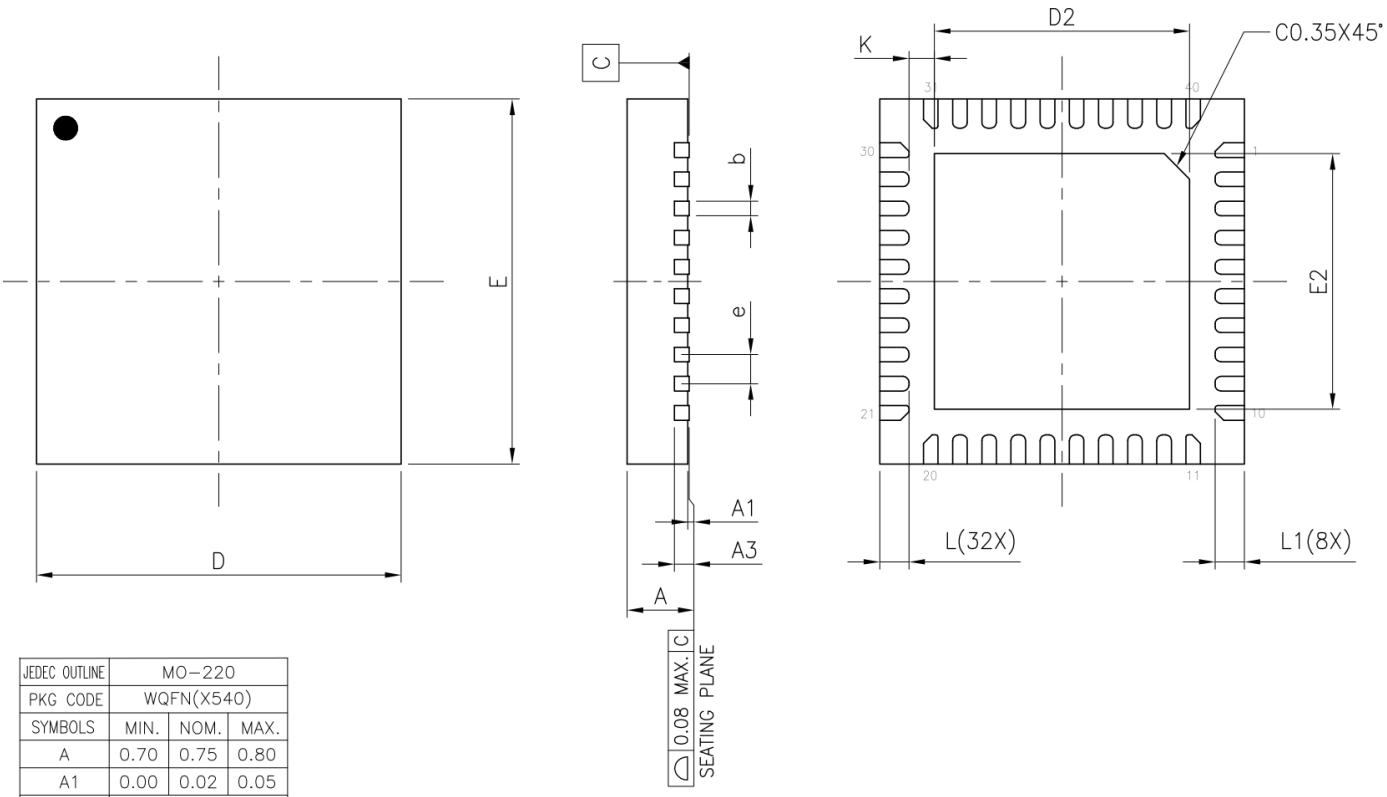


Figure 30 - ES9841 Recommended PCB Layout Guidelines

40 QFN Package Dimensions



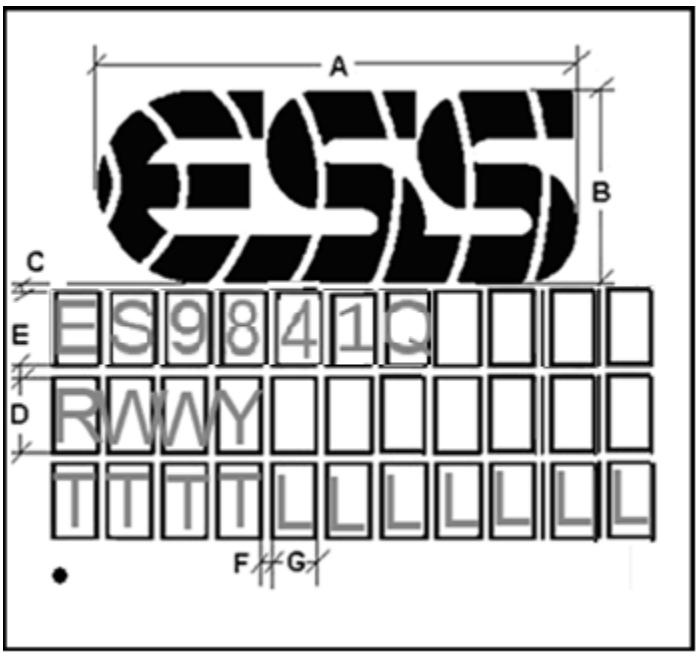
JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X540)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	5.00 BSC		
E	5.00 BSC		
e	0.40 BSC		
L	0.35	0.40	0.45
L1	0.33	0.38	0.43
K	0.20	–	–

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
A150X15R MIL	3.40	3.50	3.60	3.40	3.50	3.60	V	X	W(V)HHE-1

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 31 - ES9841 40 QFN Package Dimensions

40 QFN Top View Marking



	Dimension in mm						
Package Type	A	B	C	D	E	F	G
QFN 5mm x 5mm	4.0	1.6	0.2	0.4	0.2	0.1	0.3

T	Tracking number
W	Work week
Y	Last digit of year
L	Lot number
R	Silicon Revision

Marking is subject to change. This drawing is not to scale.

Figure 32 - ES9841 40 QFN Top View Marking

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2-Pb-Free Process - Classification Temperatures (Tc)). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

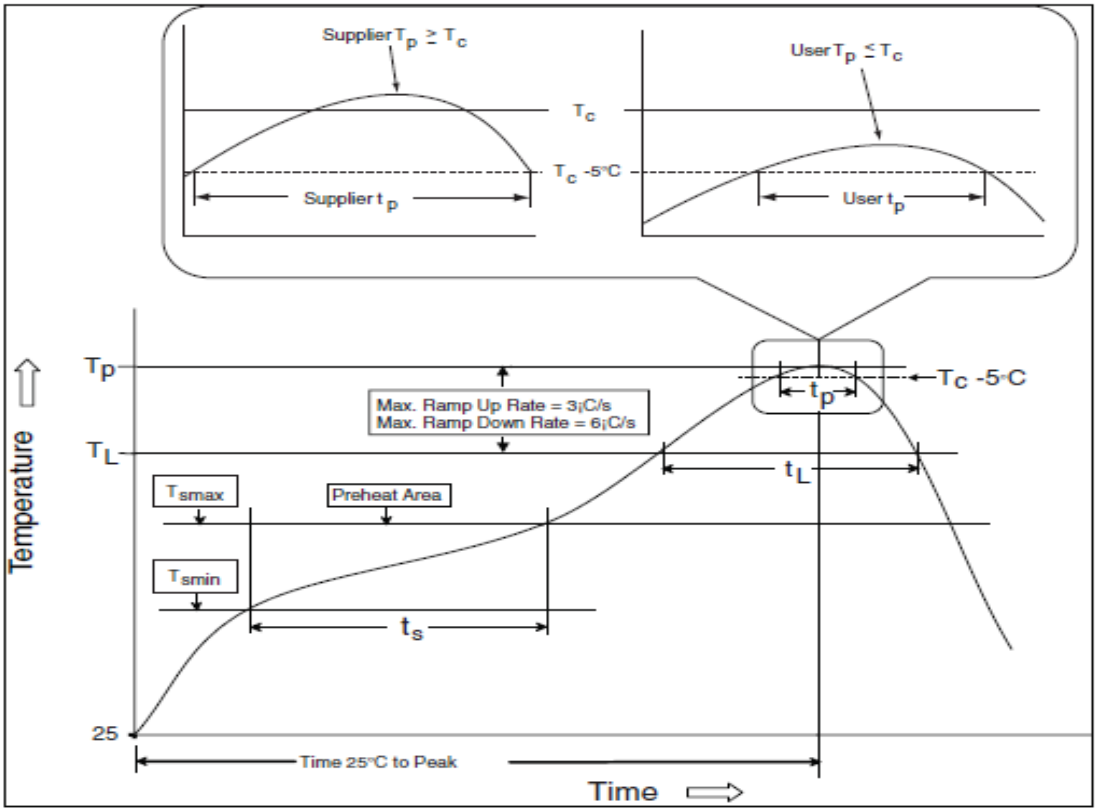


Figure 33 - IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time, bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350ºC no longer than 3 seconds.

RPC-1 Classification Reflow Profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc)	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 42 - RPC-1 Classification Reflow Profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

RPC-2 Pb-Free Process - Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 43 - RPC-2 Pb Free Classification Temperatures

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9841Q	SABRE 4 Channel High Performance 4 Channel ADC	5mm x 5mm 40 QFN

Table 44 - Ordering Information

Revision History

Current Version 0.5

Rev.	Date	Notes
0.4	November, 2025	Production release
0.5	March, 2026	• Updated BCK and WS Timing • Updated Pin Descriptions table with required capacitor notes • Updated Register 76[7, 6], 85-86[14:12, 10:8, 6:4, 2:0], 90-97, 108[0] • Correction to Register 3[1] • Fixed incorrect bit pattern for I²C Read Example • Corrected swapped pin names for Pins 27 and 28 • Updated reference schematic capacitor specifications