Analog Reinvented

ES9821

32-bit High Performance 2 Channel ADC

Product Datasheet

The SABRE® ES9821 is a 32-bit analog-to-digital (A/D) converter targeted for professional audio applications such as recording systems, mixer consoles and digital audio workstations (DAW), test equipment, instruments, audio processors, digital turntables, and consumer applications.

The ES9821 has 2 integrated ADCs which use ESS Technology's patented Hyperstream® II ADC Architecture, which delivers unprecedented audio sound quality and specifications, including a DNR of +120dB & THD+N of -112dB in 2 channel mode.

The SABRE ADC supports S/PDIF, I²S master/slave, and TDM outputs, and Hardware mode for quick configurations.

The ES9821 has built-in preprogramed filter coefficients to match perfectly with the SABRE PRO® Series of DACs including the ES9038PRO. These complimentary filters allow for analog-digital-analog processing with the upmost audio fidelity and minimized time-domain smearing.

The ES9821 has an Ultra-Low Noise Floor Bandwidth of 200kHz. This bandwidth is up to 10 times wider than the competition, enabling higher resolution at higher sample rates.

FEATURE	DESCRIPTION
+120dB DNR per Channel w/o PLL -112dB THD+N per Channel w/o PLL	Unprecedented Dynamic Range and Ultra-Low Distortion
High Sample Rates	Up to PCM 768kHz
Customizable Filter Characteristics	8 Presets of Digital Optimal Filters
Multiple Output Formats Available	PCM, TDM, and S/PDIF Outputs are Available
I²C, SPI, and Hardware Interface Control	Configured by microcontroller or other I²C/SPI master, or pins through Hardware Mode
Ultra-Low Noise Floor Bandwidth	200kHz Bandwidth Enabling Higher Resolution at Higher Sample Rates
Integrated Low Noise ADC Reference Regulators	Reduced BOM Cost, PCB Area and Improved DNR if Required
Low Power Consumption	Simplifies Power Supply Design
Low Pin Count Standardized Packaging	5mm x 5mm, 28 pin QFN

Applications

- Professional digital audio workstations Audio Recording
- Very high-quality microphones
- High quality record turntable to USB conversion

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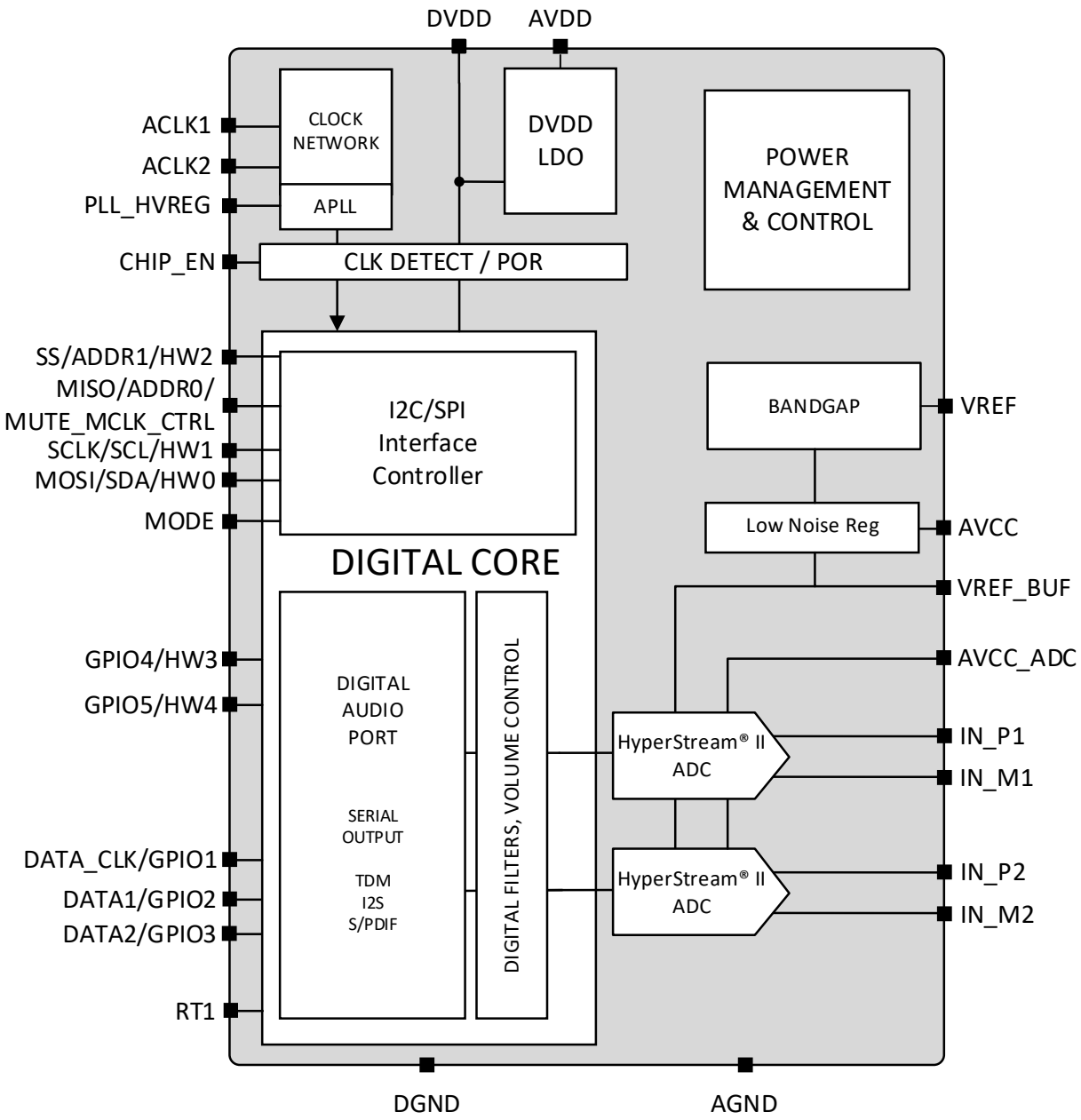
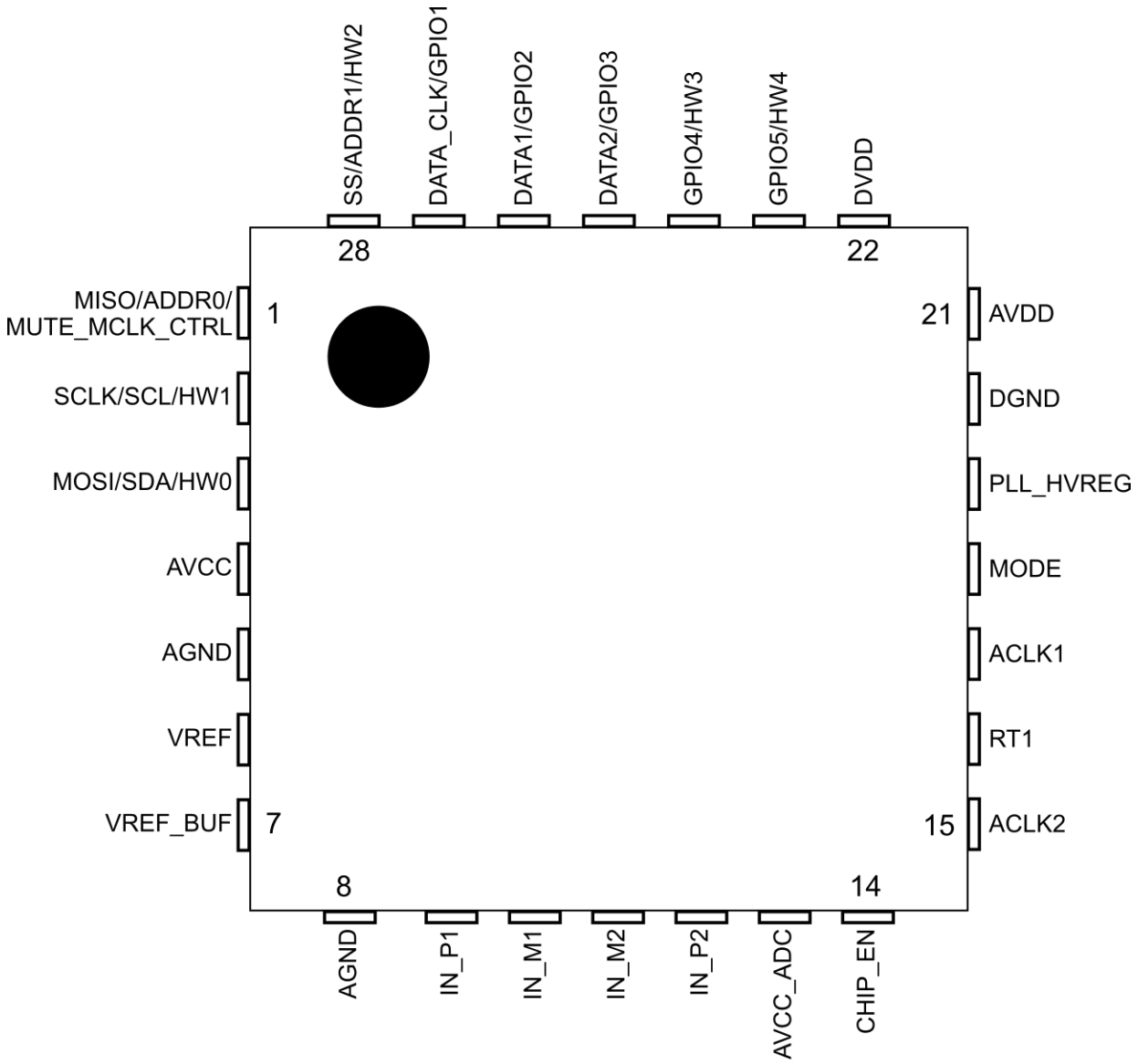


Figure 1 - ES9821 Block Diagram

ES9821Q Package

28 QFN Pinout[1]



ES9821Q
(Top View)

Figure 2 - ES9821Q 28 Pin QFN Pinout

[1] Pin 29 is a package pad and should be connected to Ground.

28 QFN Pin List

Pin	Name	Pin Type	Reset State	Pin Description
1	MISO	I/O	HiZ	SPI Main Out Sub In pin, controlled by MODE
	ADDR0			I²C Address 0 pin, controlled by MODE
	MUTE_MCLK_CTRL			Hardware Mute Control and MCLK rate set pin, controlled by MODE
2	SCLK	I/O	HiZ	SPI Serial Clock pin, controlled by MODE
	SCL			I²C Serial Clock pin, controlled by MODE
	HW1			Hardware 1 interface pin, controlled by MODE
3	MOSI	I/O	HiZ	SPI Main Out Sub In pin, controlled by MODE
	SDA			I²C Serial Data pin, controlled by MODE
	HW0			Hardware 0 interface pin, controlled by MODE
4	AVCC	Power	Power	3.3V Supply
5	AGND	Ground	Ground	Analog Ground
6	VREF	Power	Power	Low Noise reference for bandgap circuitry. Internally generated. Requires external 4.7uF decoupling capacitor to ground. See Reference Schematic for details.
7	VREF_BUF	Power	Power	Low Noise regulator output. Internally generated. Requires external 4.7uF decoupling capacitor with low ESR to ground. See Reference Schematic for details.
8	AGND	Ground	Ground	Analog Ground
9	IN_P1	AI	HiZ	ADC Channel 1 differential positive (+) input
10	IN_M1	AI	HiZ	ADC Channel 1 differential negative (-) input
11	IN_M2	AI	HiZ	ADC Channel 2 differential negative (-) input
12	IN_P2	AI	HiZ	ADC Channel 2 differential positive (+) input
13	AVCC_ADC	Power	Power	ADC reference voltage 3.3V Supply
14	CHIP_EN	I/O	HiZ	Active-high chip enable.
15	ACLK2	AI	HiZ	Auxiliary Clock Input 2
16	RT1	I	HiZ	Reserved. Must be connected to DGND for normal operation.
17	ACLK1	AI	HiZ	Auxiliary Clock Input 1
18	MODE	I/O	HiZ	I²C/SPI Control selection or HW mode

19	PLL_HVREG	Power	Power	Low Noise reference for PLL regulator. Internally generated. Requires external 1uF decoupling capacitor to ground. See Reference Schematic for details.
20	DGND	Ground	Ground	Digital Core Ground
21	AVDD	Power	Power	3.3V, I/O Supply
22	DVDD	Power	Power	Digital Core Supply. Internally generated. Requires external 1uF decoupling capacitor to ground. See Reference Schematic for details.
23	GPIO5	I/O	HiZ	General I/O w/extended functions
	HW4			Hardware 4 interface pin
24	GPIO4	I/O	HiZ	General I/O w/extended functions
	HW3			Hardware 3 interface pin
25	DATA2	I/O	HiZ	Serial DATA2
	GPIO3			General I/O w/extended functions
26	DATA1	I/O	HiZ	Serial DATA1
	GPIO2			General I/O w/extended functions
27	DATA_CLK	I/O	HiZ	Serial DATA_CLK
	GPIO1			General I/O w/extended functions
28	SS	I/O	HiZ	SPI Slave Select pin, controlled by MODE
	ADDR1			I²C Address 1 pin, controlled by MODE
	HW2			Hardware 2 interface pin, controlled by MODE
29[2]	Package PAD	-	-	Not electrically connected, used for heat dissipation

Table 1 - 28 QFN Pin List

[2] Pin 29 is the package pad. See 28 QFN Package Dimensions for sizing. Connect to DGND if desired.

Configuration Modes

The ES9821 has 4 control programming modes. They are controlled by the state of the MODE Pin (Pin 18).

Mode Pin	Configuration
0	I²C Interface
Pull Low	HW control mode (see Hardware Mode Table)
Pull High	HW control mode (see Hardware Mode Table)
1	SPI interface

Table 2 - Configuration Mode

Software Mode

The ES9821 supports both I²C or SPI serial communication to configure the registers. There are three types of registers, read/write registers, read-only registers and write-only registers. The read/write registers and the read-only registers require a system clock supplied externally or from the integrated PLL. The write-only registers are accessible through a synchronous I2C interface that does not require a system clock and allows for PLL configuration to set up a system clock.

Required Software Mode Startup Sequence

ES9821 starts up in master mode, if a clock is on ACLK1, DATA_CLK (bit clock) and DATA1 (frame clock) will drive out PCM clocks. If using the device in slave mode, the following registers need to be set immediately after CHIP_EN is asserted to avoid two masters driving clocks into the same digital serial audio bus:

1. CHIP_EN is asserted high.
2. Register 29[1:0] = 2'b00, tri-states GPIO1 and GPIO2 outputs.
3. Register 26[7:0] = 8'h11, changes GPIO1 and GPIO2 config, from 'Aux outputs' to 'Aux inputs'
4. Register 4[7:0] = 8'h00, sets the ES9821 MASTER_MODE_ENABLE = 0 for slave mode.

I²C Slave/Synchronous Slave Interface Commands

The I²C slave interface is used when the MODE Pin (Pin 18) is pulled low.

The I²C slave interface can be accessed using Pins 1, 2, 3, and 28.

- Pin 3 SDA
- Pin 2 SCL
- Pin 1 ADDR0
- Pin 28 ADDR1

The ADDR1 (Pin 28) and ADDR0 (Pin 1) determines the I²C address.

The R/W bit determines the command type, Read (1) or Write (0).

- I²C Slave Address = [5'b01000, ADDR1, ADDR0, R/W]
- I²C Synchronous Slave Address = [5'b01001, ADDR1, ADDR0, R/W]

Note: The I²C Slave interface requires an MCLK present to function, the I²C Synchronous Slave interface does not.

I²C Slave Address	I²C Synchronous Slave Address	ADDR1	ADDR0
0x40	0x48	Tie Low	Tie Low
0x42	0x4A	Tie Low	Tie High
0x44	0x4C	Tie High	Tie Low
0x46	0x4E	Tie High	Tie High

Table 3 - I²C Slave/Synchronous Slave Addresses

See I²C Slave/Synchronous Slave Interface Timing for timing information.

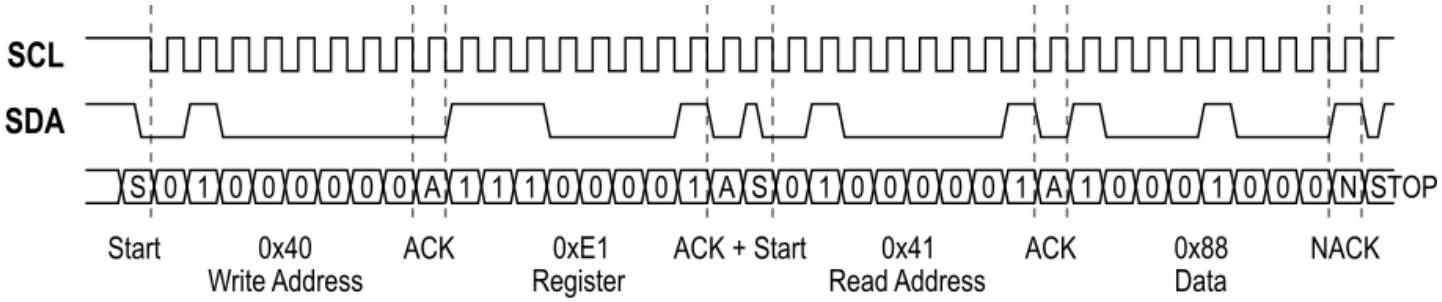


Figure 3 - I²C Read Example

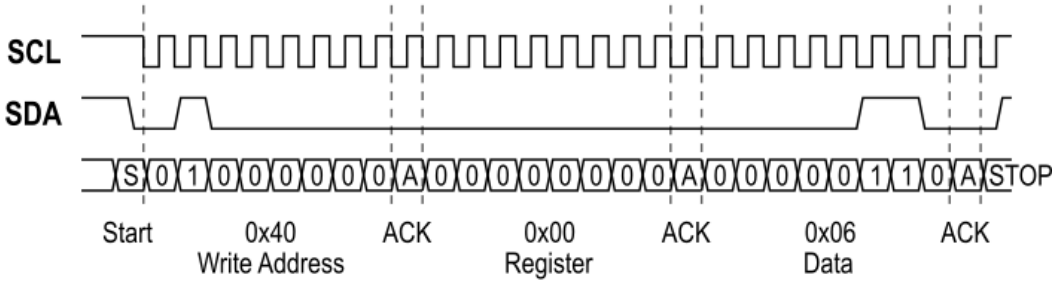


Figure 4 - I²C Write Example

SPI Slave Interface Commands

The SPI Slave interface is used when the MODE Pin (Pin 18) is pulled high.

The SPI slave interface can be accessed using Pins 1, 2, 3, and 28.

- Pin 2 SCLK
- Pin 28 SS
- Pin 3 MOSI
- Pin 1 MISO

The 4-wire SPI data format is: Command (1 byte) + Address (1 byte) + Data.

SPI commands:

- 0x01: Read
- 0x03: Write
- 0x07: Write-only Register Addresses 192-203 (0xC0 - 0xCB)

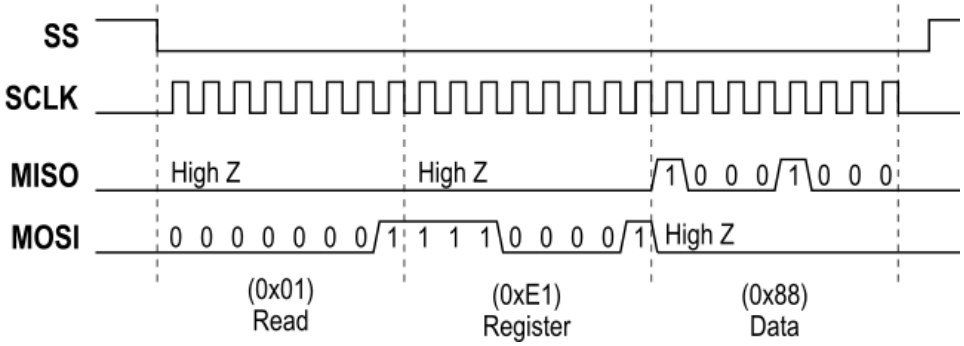


Figure 5 - SPI Single Byte Read

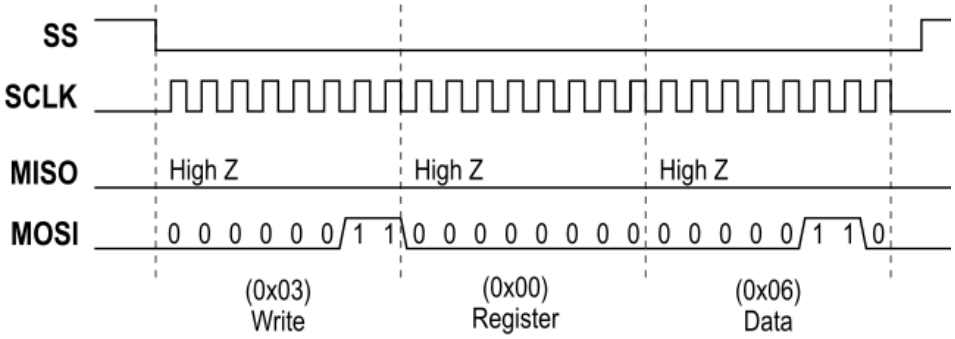


Figure 6 - SPI Single Byte Write

Hardware Mode

The ES9821 has pre-configured modes that can be set with external pin configuration. These modes configure the ADC for different serial data rates and set the ADC muting.

All Hardware modes use ACLK1 and use the default Minimum Phase digital filter.

These modes are set with pins:

- MODE (pin 18)
- HW0 (pin 3)
- HW1 (pin 2)
- HW2 (pin 28)
- HW3 (pin 24)
- HW4 (pin 23)

Each hardware mode pin has 4 states:

- 0 - Pin directly connected to GND
- 1 - Pin directly connected to AVDD
- Pull 0 - Pin pulled to GND through 47kΩ resistor
- Pull 1 - Pin pulled to AVDD through 47kΩ resistor

Design Information

Hardware pins can be configured in 4 different ways. Each pin can be tied-high (1), pulled-high (Pull 1), pulled-low (Pull 0), or tied-low (0). HW0 and HW1 pins are always tied-high or tied-low. These 4 options also apply to MUTE_MCLK_CTRL.

The HW0 and HW1 pins never require a pull-high or pull-low resistor.

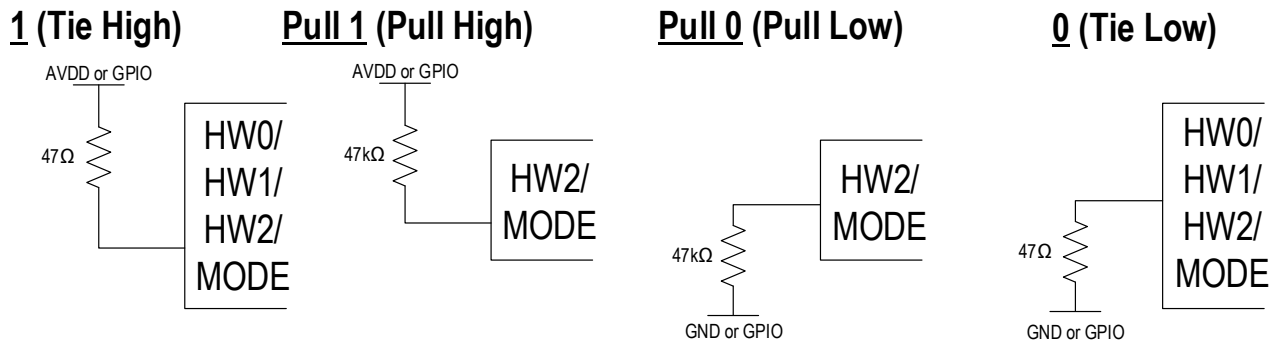


Figure 7 - Hardware Mode Pin Configurations

Muting

MUTE_MCLK_CTRL (Pin 1) is used to control the muting of the output and MCLK rate while in Hardware Mode:

- 0 - Mute, 24.576MHz / 22.579MHz
- 1 - Unmuted, 24.576MHz / 22.579MHz
- Pull 0 - Mute, 49.152MHz / 45.158MHz
- Pull 1 - Unmuted, 49.152MHz / 45.158MHz

DC Blocking

GPIO4/HW3 (Pin 24) is used to control the ADC's DC Blocking feature while in Hardware Mode:

- 0 - DC blocking disabled
- 1 - DC blocking enabled

S/PDIF

In hardware modes #4-7, S/PDIF is encoded and output from GPIO5/HW4 in addition to the Left Justified data on the digital serial port (DCLK, DATA1, DATA2)

TDM Channel Mapping

In TDM hardware modes, ES9821 supports 4 channels, 8 channels, 16 channels and up to 32 channels per data line through autodetection. For 32 channels, GPIO5/HW4 is used to add 16 to the channel mapped. For example, Hardware modes 16 and 32 are the same hardware configuration except for GPIO5/HW4; HW mode 16 maps the outputs to slots 1 and 2, while HW mode 32 maps the outputs to slots 16 and 17.

Hardware Mode Pin Configurations

HW Mode	FS (kHz)	BCK (MHz)	MCLK (MHz)	BCK/Channel	Channel Slots	MODE	HW2	HW1	HW0
I²S Master Mode, Ext MCLK									
0	MCLK / 128	MCLK / 2	24.576/49.152	32	1,2	Pull 0	0	0	0
1	MCLK / 256	MCLK / 4	24.576/49.152	32	1,2	Pull 0	0	0	1
2	MCLK / 512	MCLK / 8	24.576/49.152	32	1,2	Pull 0	0	1	0
3	MCLK / 1024	MCLK / 16	24.576/49.152	32	1,2	Pull 0	0	1	1
LJ Master, EXT MCLK (with S/PDIF enabled on GPIO5/HW4)									
4	MCLK / 128	MCLK / 2	24.576/49.152	32	1,2	Pull 0	Pull 0	0	0
5	MCLK / 256	MCLK / 4	24.576/49.152	32	1,2	Pull 0	Pull 0	0	1
6	MCLK / 512	MCLK / 8	24.576/49.152	32	1,2	Pull 0	Pull 0	1	0
7	MCLK / 1024	MCLK / 16	24.576/49.152	32	1,2	Pull 0	Pull 0	1	1
I²S Slave, Ext MCLK, AutoDetect FS and BCK									
8	8 < FS ≤ 384	64FS	24.576/49.152	32	1,2	Pull 0	Pull 1	0	0
LJ Slave, AutoDetect FS and BCK									
12	8 < FS ≤ 384	64FS	24.576/49.152	32	1,2	Pull 0	1	0	0
TDM Left Justified Slave, Autodetect FS and BCK, GPIO5/HW4 =0									
16	8 < FS ≤ 384	Auto (64FS, 128FS, 256FS, 512FS, 1024FS)	24.576/49.152	32	1,2	Pull 1	0	0	0
17	8 < FS ≤ 384	Auto (128FS, 256FS, 512FS, 1024FS)	24.576/49.152	32	3,4	Pull 1	0	0	1
18	8 < FS ≤ 384	Auto (256FS, 512FS, 1024FS)	24.576/49.152	32	5,6	Pull 1	0	1	0
19	8 < FS ≤ 384	Auto (256FS, 512FS, 1024FS)	24.576/49.152	32	7,8	Pull 1	0	1	1
20	8 < FS ≤ 384	Auto (512FS, 1024FS)	24.576/49.152	32	9,10	Pull 1	Pull 0	0	0
21	8 < FS ≤ 384	Auto (512FS, 1024FS)	24.576/49.152	32	11,12	Pull 1	Pull 0	0	1
22	8 < FS ≤ 384	Auto (512FS, 1024FS)	24.576/49.152	32	13,14	Pull 1	Pull 0	1	0
23	8 < FS ≤ 384	Auto (512FS, 1024FS)	24.576/49.152	32	15,16	Pull 1	Pull 0	1	1
TDM Left Justified Slave, Autodetect FS and BCK, GPIO5/HW4 =0									
24	8 < FS ≤ 384	Auto (32FS, 64FS, 128FS, 256FS, 512FS)	24.576/49.152	16	1,2	Pull 1	Pull 1	0	0

25	8 < FS ≤ 384	Auto (64FS, 128FS, 256FS)	24.576/49.152	16	3,4	Pull 1	Pull 1	0	1
26	8 < FS ≤ 384	Auto (128FS, 256FS, 512FS)	24.576/49.152	16	5,6	Pull 1	Pull 1	1	0
27	8 < FS ≤ 384	Auto (128FS, 256FS, 512FS)	24.576/49.152	16	7,8	Pull 1	Pull 1	1	1
28	8 < FS ≤ 384	Auto (256FS, 512FS)	24.576/49.152	16	9,10	Pull 1	1	0	0
29	8 < FS ≤ 384	Auto (256FS, 512FS)	24.576/49.152	16	11,12	Pull 1	1	0	1
30	8 < FS ≤ 384	Auto (256FS, 512FS, 1024FS)	24.576/49.152	16	13,14	Pull 1	1	1	0
31	8 < FS ≤ 384	Auto (256FS, 512FS)	24.576/49.152	16	15,16	Pull 1	1	1	1
TDM Left Justified Slave, Autodetect FS and BCK, GPIO5/HW4 = 1									
32	8 < FS ≤ 384	Auto (1024FS)	24.576/49.152	32	17,18	Pull 1	0	0	0
33	8 < FS ≤ 384	Auto (1024FS)	24.576/49.152	32	19,20	Pull 1	0	0	1
34	8 < FS ≤ 384	Auto (1024FS)	24.576/49.152	32	21,22	Pull 1	0	1	0
35	8 < FS ≤ 384	Auto (1024FS)	24.576/49.152	32	23,24	Pull 1	0	1	1
36	8 < FS ≤ 384	Auto (1024FS)	24.576/49.152	32	25,26	Pull 1	Pull 0	0	0
37	8 < FS ≤ 384	Auto (1024FS)	24.576/49.152	32	27,28	Pull 1	Pull 0	0	1
38	8 < FS ≤ 384	Auto (1024FS)	24.576/49.152	32	29,30	Pull 1	Pull 0	1	0
39	8 < FS ≤ 384	Auto (1024FS)	24.576/49.152	32	31,32	Pull 1	Pull 0	1	1
TDM Left Justified Slave, Autodetect FS and BCK, GPIO5/HW4 = 1									
40	8 < FS ≤ 384	Auto (512FS)	24.576/49.152	16	17,18	Pull 1	Pull 1	0	0
41	8 < FS ≤ 384	Auto (512FS)	24.576/49.152	16	19,20	Pull 1	Pull 1	0	1
42	8 < FS ≤ 384	Auto (512FS)	24.576/49.152	16	21,22	Pull 1	Pull 1	1	0
43	8 < FS ≤ 384	Auto (512FS)	24.576/49.152	16	23,24	Pull 1	Pull 1	1	1
44	8 < FS ≤ 384	Auto (512FS)	24.576/49.152	16	25,26	Pull 1	1	0	0
45	8 < FS ≤ 384	Auto (512FS)	24.576/49.152	16	27,28	Pull 1	1	0	1
46	8 < FS ≤ 384	Auto (512FS)	24.576/49.152	16	29,30	Pull 1	1	1	0
47	8 < FS ≤ 384	Auto (512FS)	24.576/49.152	16	31,32	Pull 1	1	1	1

Table 4 - Hardware Mode Configurations

Note 1: In 352.8kHz/384kHz sampling, modes 8,12,16-47 will require a 45.1584Mhz (44.1kHz sampling multiple) or 49.152MHz (48kHz) clock for a 128FS ratio (MCLK/FS ratio).

Note 2: MCLK is shown with a 48kHz clock. If 44.1kHz ratios are required, a clock of 22.5792Mhz/45.1584Mhz should be used.

Required Hardware Mode Startup Sequence

The hardware mode setup sequence is shown below with all hardware pins being defined after CHIP_EN is asserted.

Note: It is recommended that MUTE_CTRL is set low until the HW mode is finalized, then asserted last.

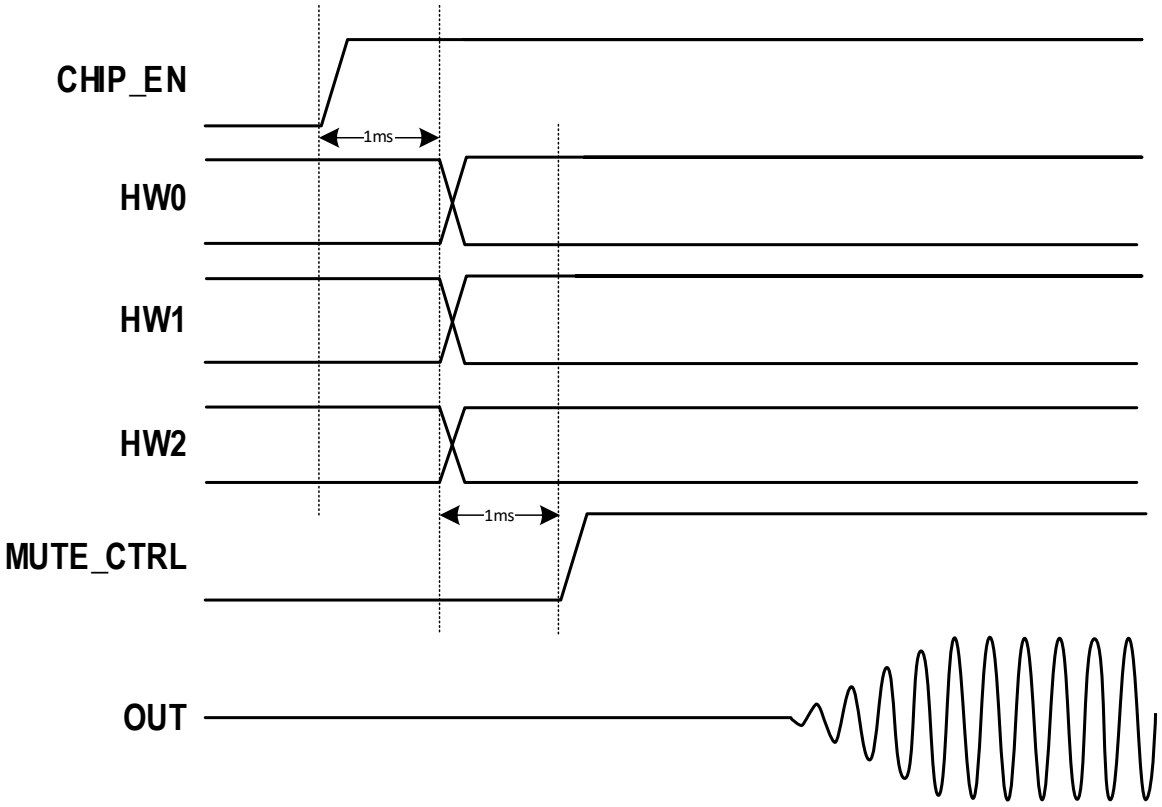


Figure 8 - Hardware Mode Startup Sequence

Digital Features

Digital Signal Path

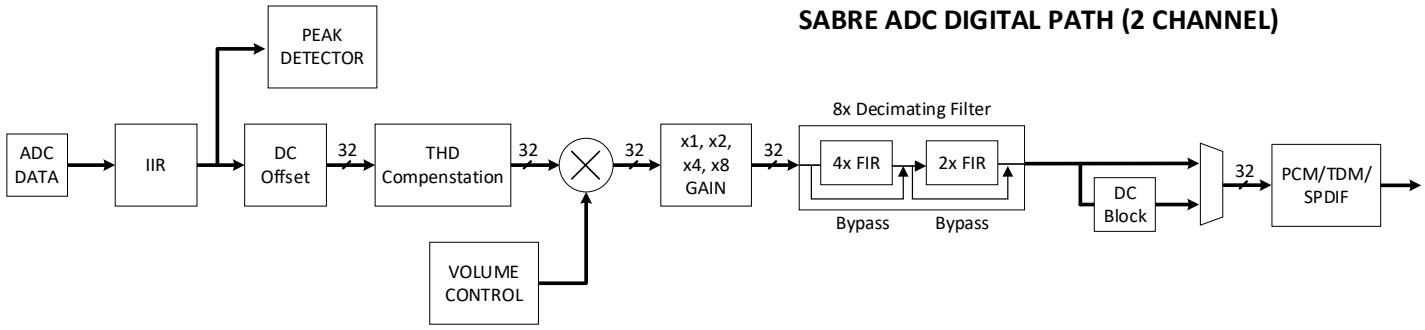


Figure 9 - Digital Signal Path

Audio Output Formats

PCM

PCM modes include the subset of I²S and Left-Justified (LJ) modes. These modes are set to carry 2 channels of converted data per digital data line, along with 2 lines of audio clocks, the bit clock, and frame clock.

To enable 16-bit output, Register 63[1:0] ENABLE_16BIT_CHx must be set.

To enable 32-bit output, Register 64[1:0] ENABLE_32BIT_CHx and Register 42[1:0] ADC_ENABLE_DC_BLOCK_CHx must be set.

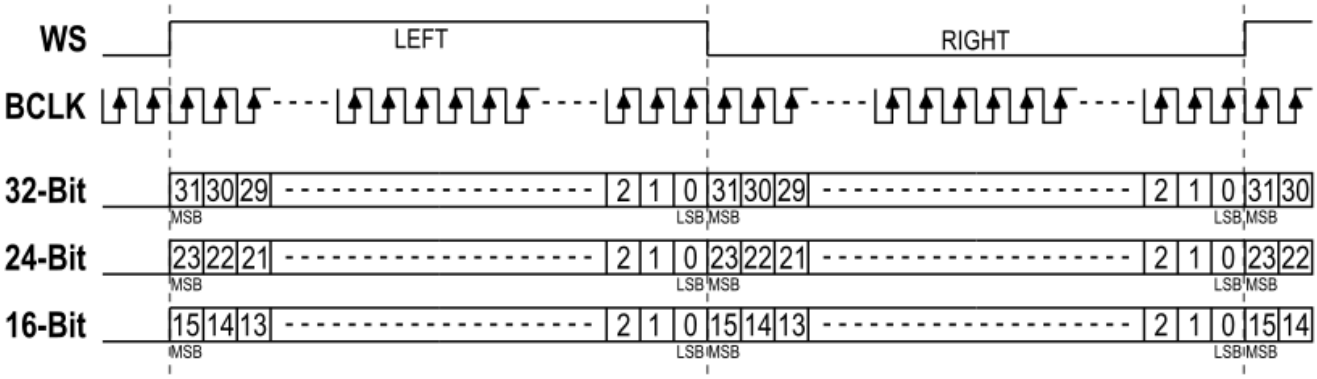


Figure 10 - Left Justified (LJ) Subset of PCM Mode

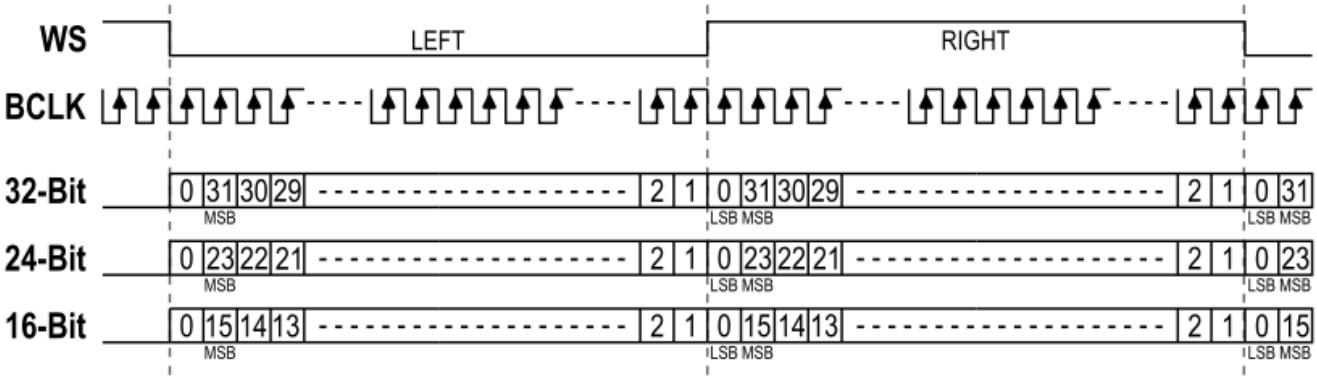


Figure 11 - I²S Subset of PCM mode

TDM

In TDM modes, several ES9821 are used in parallel to increase the number of channels. Examples of TDM128 and TDM256 are shown below with a single 4 channel and 8 channel data line, respectively. Each ES9821 can be configured in HW or SW mode to output its data to different slots on the TDM DATA line.

Note: In hardware modes, only Left Justified TDM formats are supported. In software mode, the user can configure it to be I²S TDM format.

Note: The number proceeding TDM in the format is the number of BCK cycles per frame.
Example: TDM128 has 4 Channels * 32BCK/Ch = 128 BCK/Ch

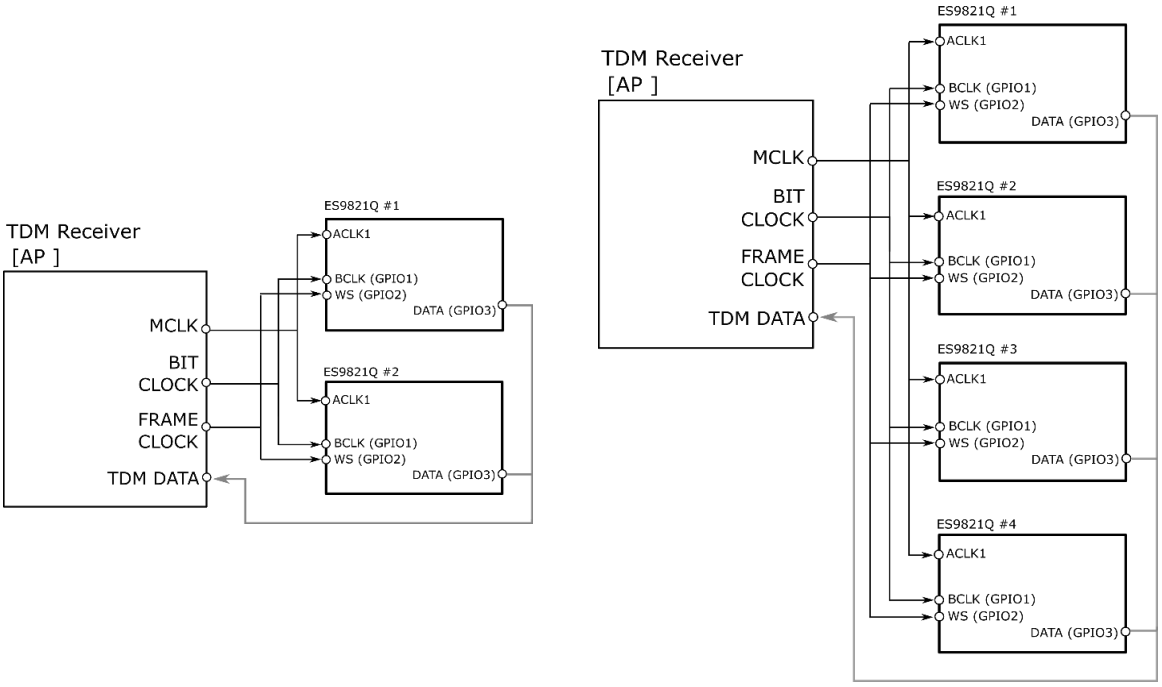


Figure 12 - TDM Connection of Several ES9821 Devices in Parallel

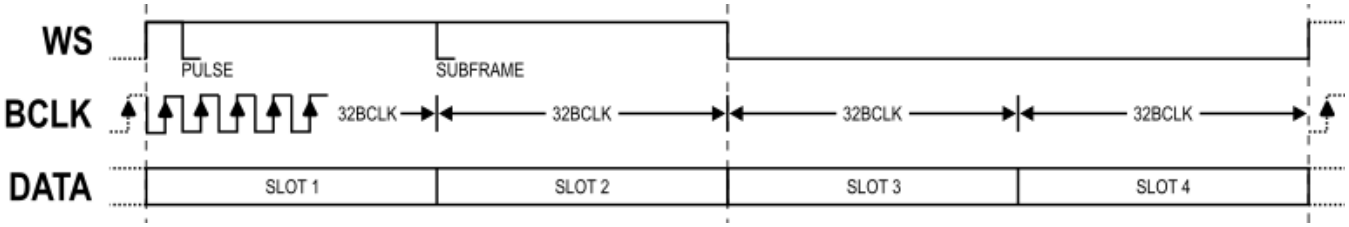


Figure 13 - TDM128 Mode

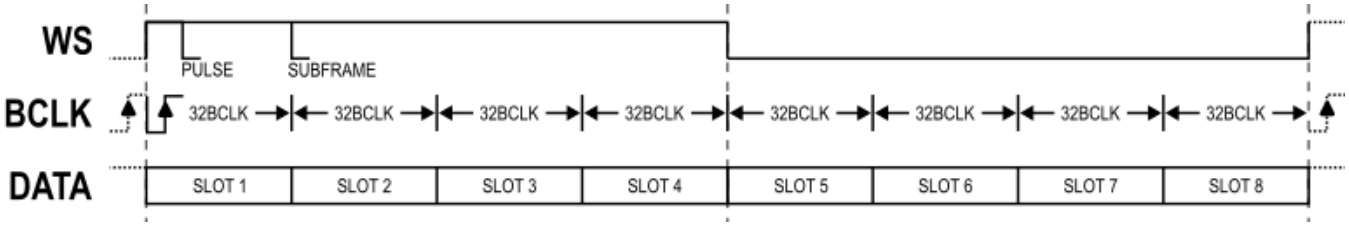


Figure 14 - TDM256 Mode

S/PDIF

S/PDIF is transmitted over a single signal line using dual phase encoded data, which allows for clock extraction from the data signal line.

The ES9821 has an integrated S/PDIF Encoder that can be accessed in Hardware Modes 4 through 7 and in Software Mode.

- For Hardware mode, the S/PDIF output is GPIO5/HW4 in HW modes 4-7
    - S/PDIF can be output at the same time as Left Justified data on the DCLK, DATA1, DATA2
- For Software mode, the applicable registers are:
    - Register 0[3] ENABLE_SPDIF_ENCODE
        - Enables S/PDIF encoder
    - Register 13-17 SPDIF CONFIG
        - Configures S/PDIF sub-code bits
    - Register 26-28 GPIOx CONFIG
        - Selects the S/PDIF output pin
    - Register 20[1] AUTO_FIR_SYNC = 1'b1
        - Must be set to 1'b1 when using without a frame clock (WS) on DATA1
        - Can be manually resynced by toggling Register 18[4] FORCE_FIR_SYNC

GPIO Configuration[3]

GPIO#_CFG	Function	I/O Direction
0	Analog Shutdown	Shutdown (default)
1	Aux Inputs	Inputs
2	Aux Outputs	Output
3	PLL_CLK_AVALID	Output
4	PLL_LOCKED	Output
5	Ch1_PEAK_INTERRUPT	-
6	Ch2_PEAK_INTERRUPT	-
7	INTERRUPT (OR of all interrupts)	-
8	S/PDIF Data Output	Output
9	PWM1	Output
10	PWM2	Output
11	PWM3	Output
12	RESERVED	Output
13	CLK ADC	Output
14	1'b0	Output
15	1'b1	Output

Table 5 - Standard GPIO Functions

For configuring pins as Inputs, Outputs, or Input/Outputs:

- Input pin
  - GPIOxx_IE = 1'b1 (Input Enable), Registers 31-29
  - GPIOxx_OE = 1'b0 (Output Enable), Registers 31-29
- Output pin
  - GPIOxx_IE = 1'b0
  - GPIOxx_OE = 1'b1
- In/Out pin (Master Mode)
  - GPIOxx_IE = 1'b1
  - GPIOxx_OE = 1'b1

In Master mode GPIO1 & GPIO 2 should be configured as In/Out pins

[3] GPIOs can be configured using Registers 26-31

Interrupts

Interrupts are enabled using individual configuration registers specific to the interrupt function. For example, the Peak Detection interrupt is enabled via Register 43 ADC_PEAK_DETECTOR_CONFIG.

Once set, interrupts must be manually cleared via Register 12 INTERRUPT.

Register 12 INTERRUPT also allows for masking of the interrupt flag bits in Register 224 READ_SYSTEM_REGISTER_0.

Interrupts can be mapped to GPIO pins using Registers 26-28 GPIO_x/x_CONFIG.

THD Compensation

THD Compensation minimizes the non-linearities of the ADCs and the input stage overall by adding second order and third order terms:

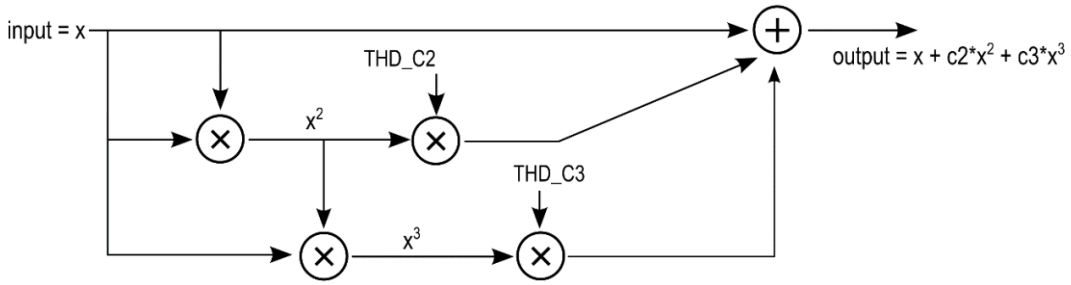


Figure 15 - TDM Compensation

The ES9821 can help compensate for system second and third harmonic distortion. In hardware mode, the coefficients CH1_C2 = CH2_C2 = 6 and CH1_C3=CH2_C3=-13 are used, as they were best to minimize any distortion at large amplitudes.

THD compensation is always enabled but if register values are zero, it will be bypassed.

- Register 56-55: THD COMP C2 CH1
- Register 58-57: THD COMP C3 CH1
- Register 60-59: THD COMP C2 CH2
- Register 62-61: THD COMP C3 CH2

For best results, compensation coefficients should be tuned for each device in-situ.

Digital Filters

The ES9821 has 8 pre-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates. (See Register 64[4:2] FILTER_SHAPE for configuration)

#	Filter	Description
1	Minimum Phase (default)	Version 2 of minimum phase fast roll-off (#6) with less ripple and more image rejection
2	Linear Phase Apodizing Fast Roll-Off	Full image rejection by FS/2 to avoid any aliasing, with smooth roll-off starting before 20k.
3	Linear Phase Fast Roll-Off	Sabre legacy filter, optimized for image rejection @ 0.55FS
4	Linear Phase Fast Roll-Off Low-Ripple	Sabre legacy filter, optimized for in-band ripple
5	Linear Phase Slow Roll-Off	Sabre legacy filter, optimized for lower latency, but symmetric impulse response
6	Minimum Phase Fast Roll-Off	Low latency, minimal pre ringing and low passband ripple, image rejection @ 0.55FS
7	Minimum Phase Slow Roll-Off	Lowest latency at the cost of image rejection
8	Minimum Phase Fast Roll-Off Low Dispersion	Provides a nice balance of the low latency of minimum phase filters and the low dispersion of linear phase filters. Minimal pre-ringing is added to achieve the low dispersion in the audio band.

Table 6 - Pre-Programmed Digital Filter Descriptions

Note: Minimum phase filters are asymmetric filters that work to minimize the pre-echo of the filter, while still maintaining an excellent frequency response and they peak earlier than linear phase filters, resulting in a lower group delay. Minimum phase filters usually feature zero cycles of pre-echo, which can result in improved audio quality.

PCM Filter Latency

The following tables show the simulated latency of each filter at a sampling rate range of 44.1/48kHz to 352.8/384kHz. Measurements were taken from the external impulse response prior to being down sampled to 1FS. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

Filter Shape \ Frequency [kHz]	44.1 / 48	88.2 / 96	176.4 / 192	352.8 / 384
Minimum Phase (default)	4.77 / FS	4.92 / FS	5.08 / FS	6.29 / FS
Linear Phase Apodizing Fast Roll-Off	34.77 / FS	34.79 / FS	35.96 / FS	36.16 / FS
Linear Phase Fast Roll-Off	34.90 / FS	34.92 / FS	36.08 / FS	36.29 / FS
Linear Phase Fast Roll-Off Low-Ripple	34.40 / FS	34.54 / FS	35.71 / FS	35.92 / FS
Linear Phase Slow Roll-Off	7.40 / FS	7.42 / FS	8.58 / FS	8.79 / FS
Minimum Phase Fast Roll-Off	4.90 / FS	4.92 / FS	5.95 / FS	6.29 / FS
Minimum Phase Slow Roll-Off	3.90 / FS	3.92 / FS	4.92 / FS	5.29 / FS
Minimum Phase Slow Roll-Off Low Dispersion	13.77 / FS	13.79 / FS	14.96 / FS	15.16 / FS

Table 7 - PCM Filter Latency

PCM Filter Properties

Minimum Phase					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-87.23 dB	0.55 FS			Hz
Group Delay		2.89/FS		9.23/FS	s
Flatness (ripple)	0.0042				dB

Linear Phase Apodizing					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.41 FS	Hz
Stop band	-82.32 dB	0.50 FS			Hz
Group Delay			33.25/FS		s
Flatness (ripple)	0.0046				dB

Linear Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-88.14 dB	0.54 FS			Hz
Group Delay			33.38/FS		s
Flatness (ripple)	0.0047				dB

Linear Phase Fast Roll-Off Low Ripple					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-77.81 dB	0.55 FS			Hz
Group Delay			33.00/FS		s
Flatness (ripple)	0.0032				dB

Linear Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.50 FS	Hz
Stop band	-84.07 dB	0.81 FS			Hz
Group Delay			5.86/FS		s
Flatness (ripple)					dB

Minimum Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-88.26 dB	0.54 FS			Hz
Group Delay		2.89/FS		9.23/FS	s
Flatness (ripple)	0.0039				dB

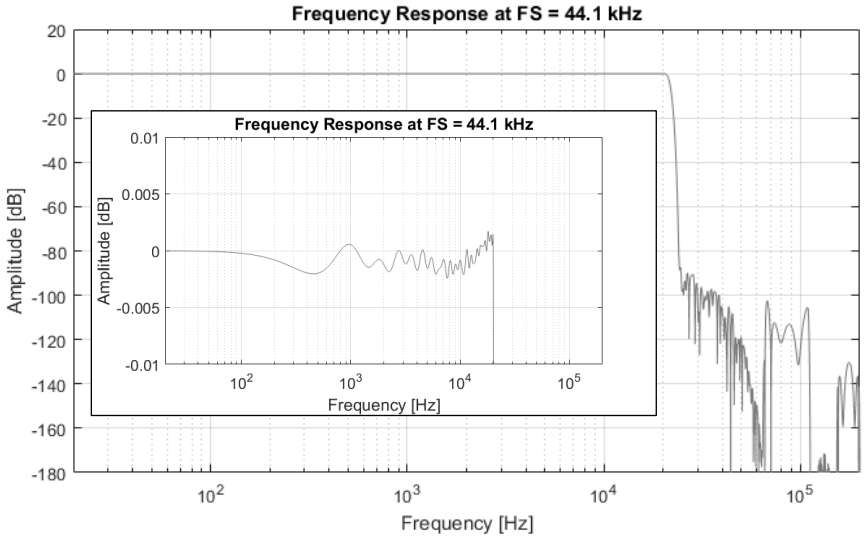
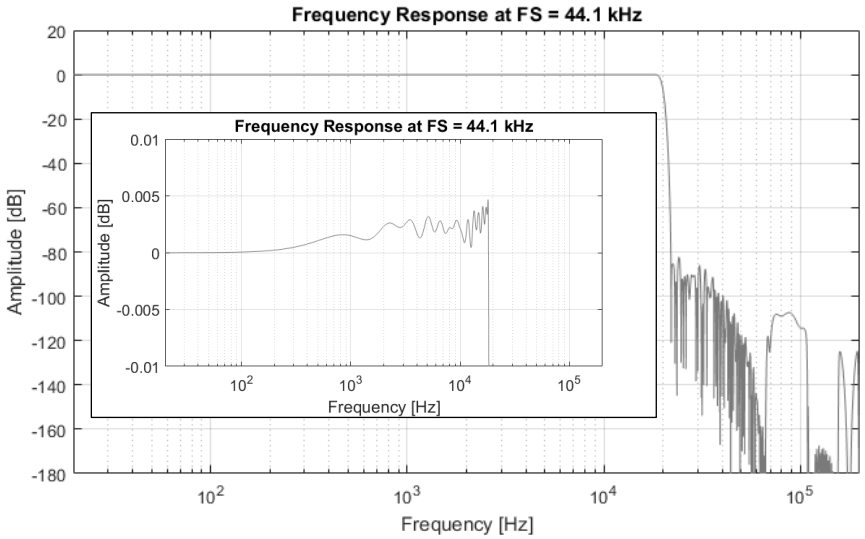
Minimum Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.43 FS	Hz
Stop band	-89.28 dB	0.80 FS			Hz
Group Delay		2.03/FS		3.50/FS	s
Flatness (ripple)					dB

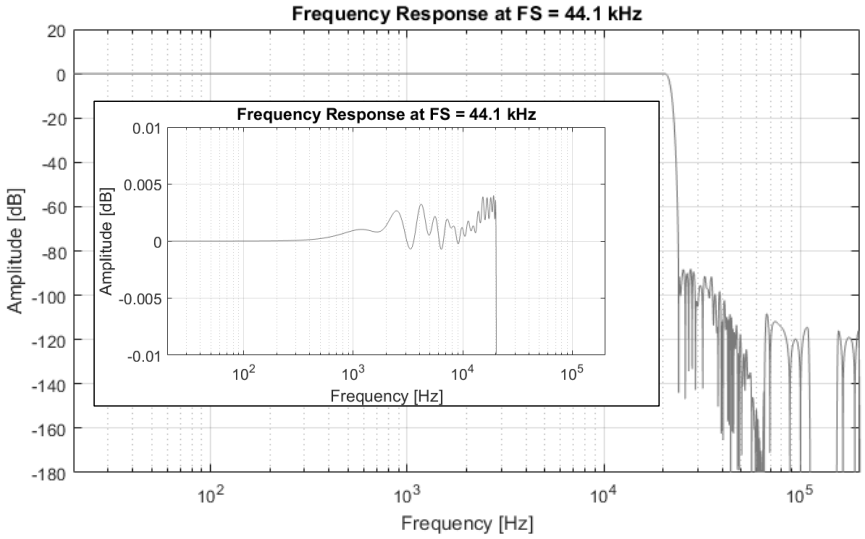
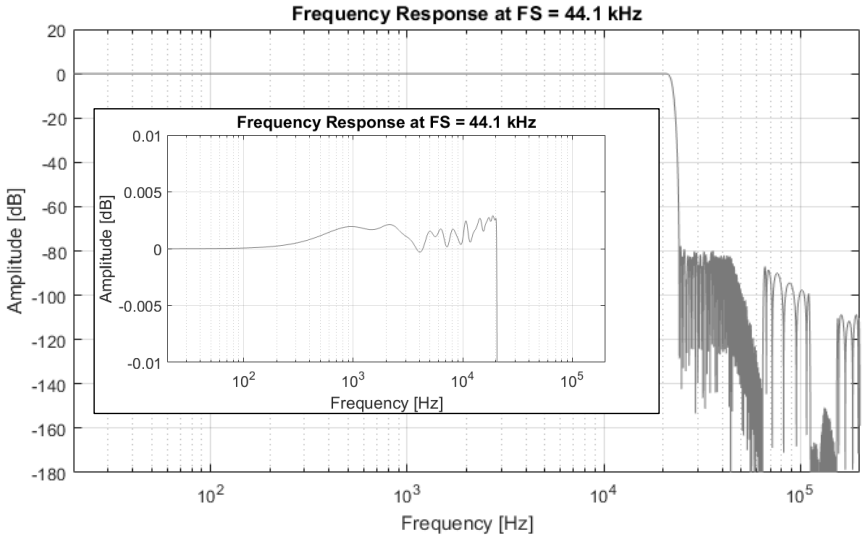
Minimum Phase Slow Roll-Off Low Dispersion					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.43 FS	Hz
Stop band	-89.28 dB	0.79 FS			Hz
Group Delay		12.13/FS		12.37/FS	s
Flatness (ripple)					dB

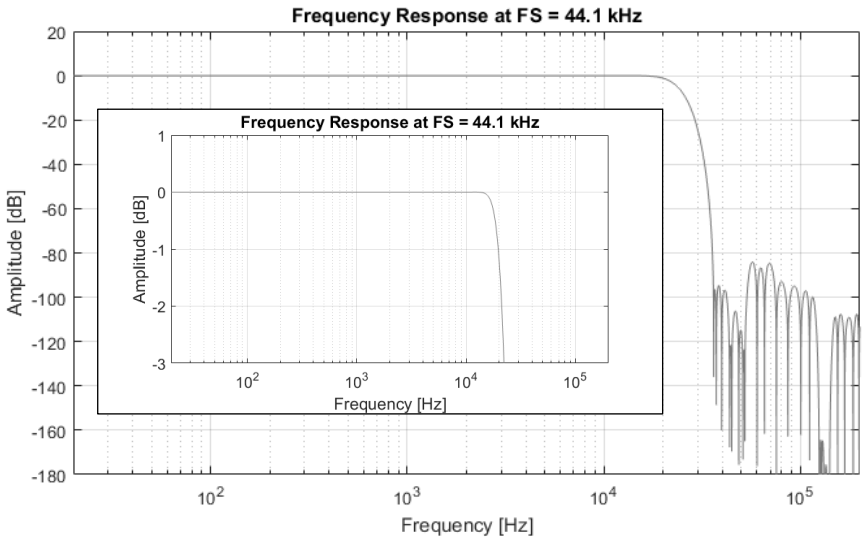
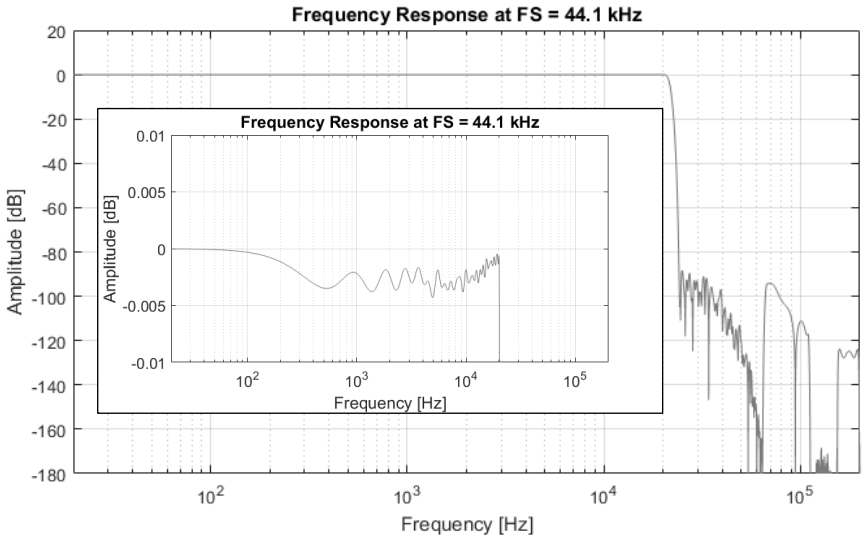
Table 8 - PCM Filter Properties

PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Frequency Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

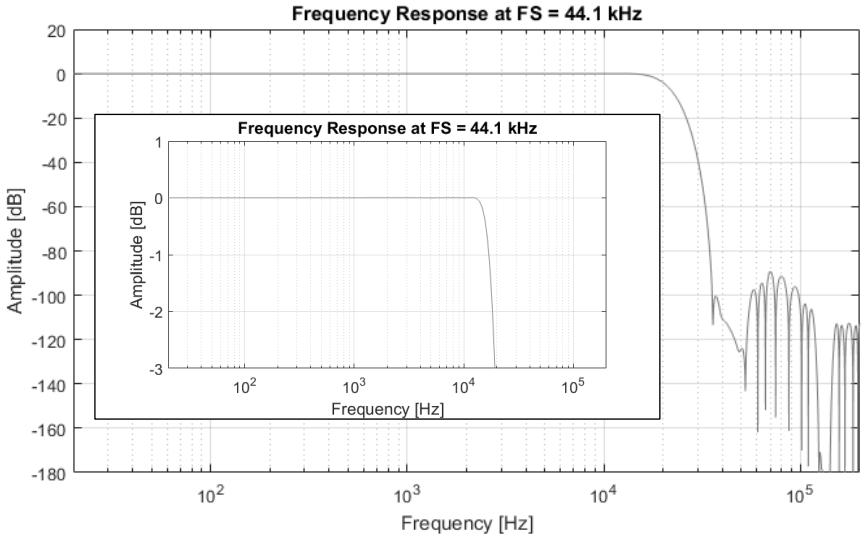
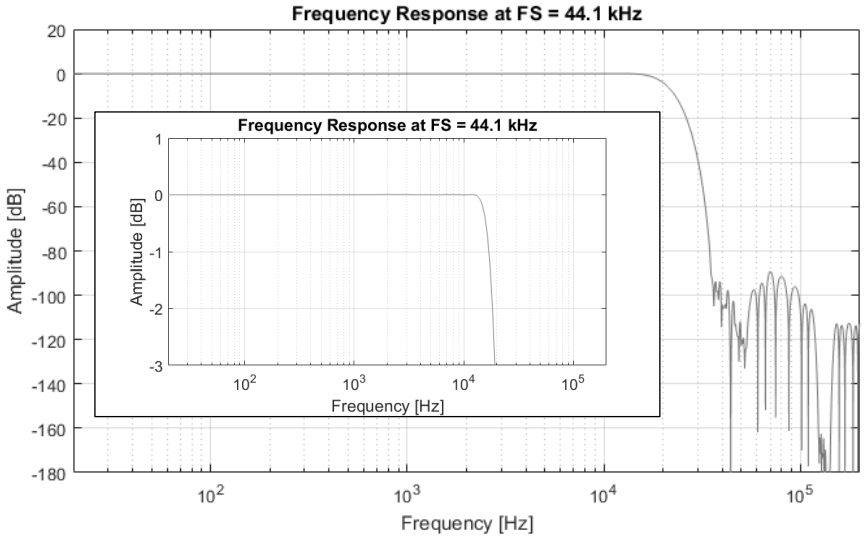
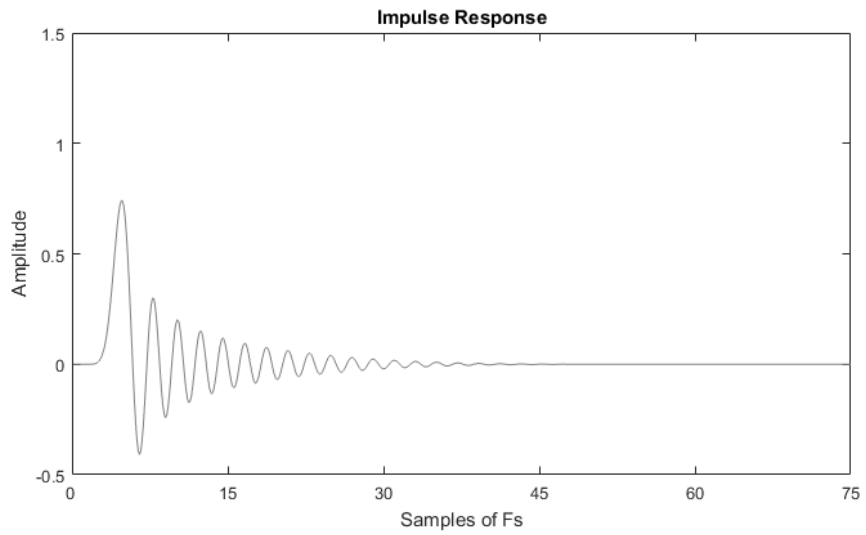
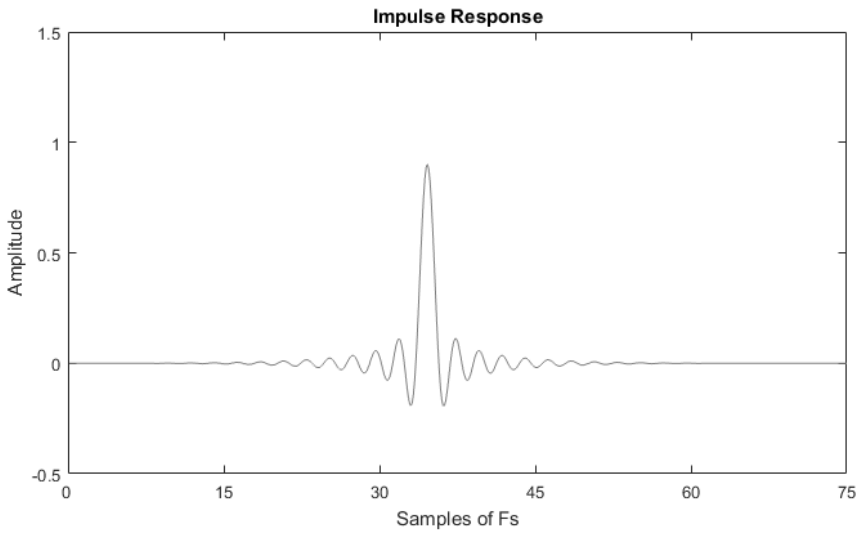
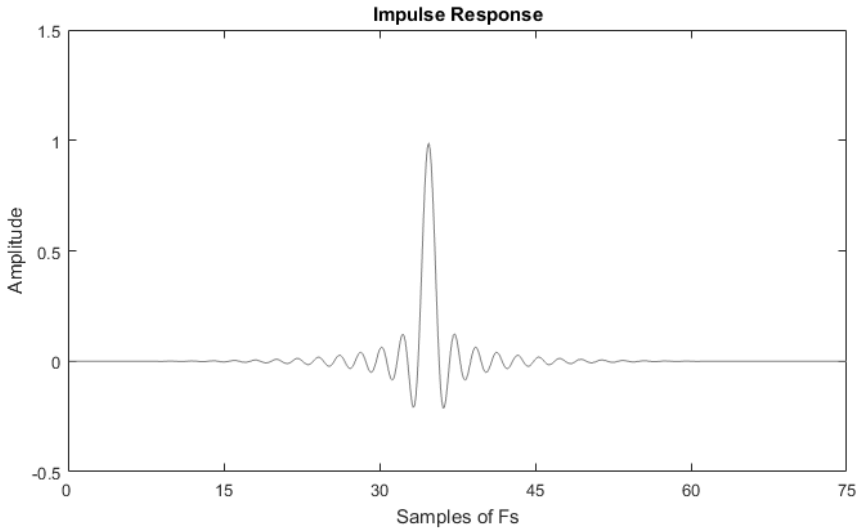
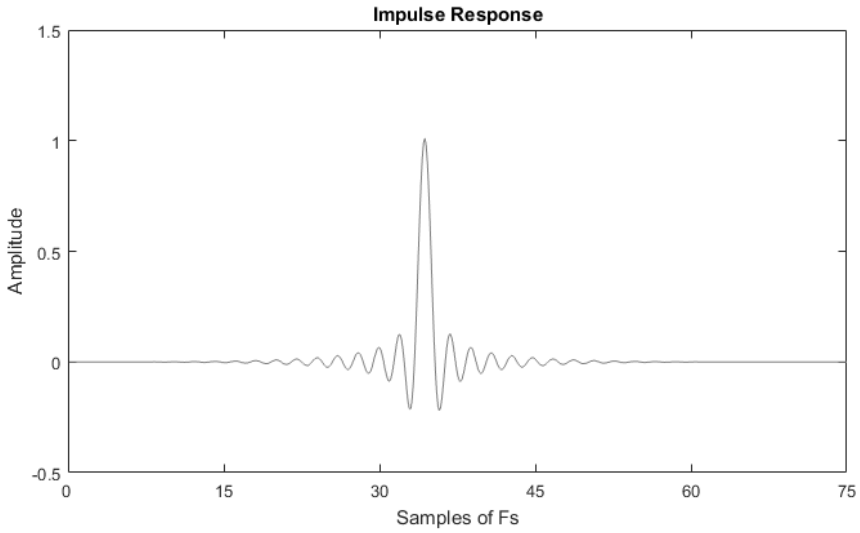
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

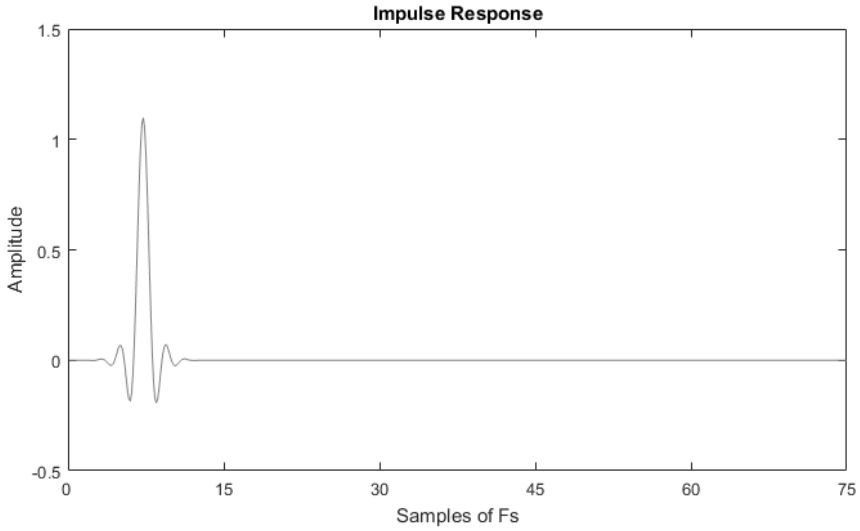
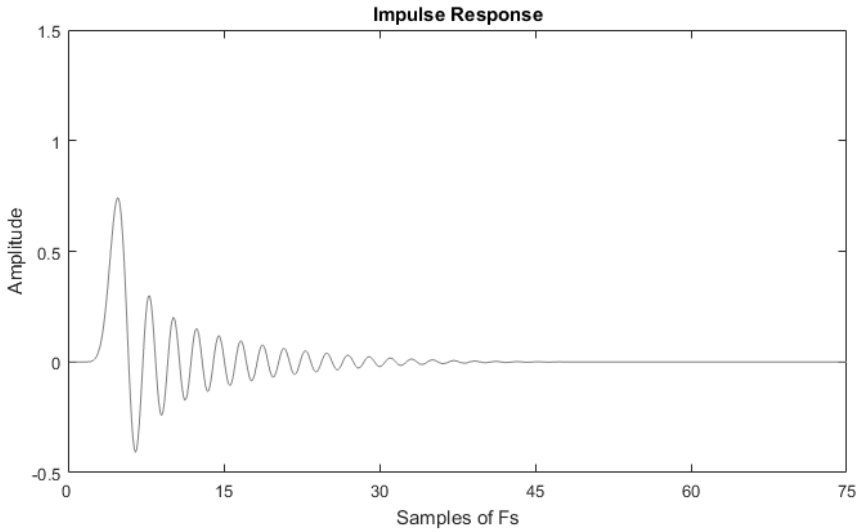
Table 9 - PCM Filter Frequency Response

PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. They show the decimation path prior to down-sampling to 1FS and are scaled accordingly. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

Filter	Impulse Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

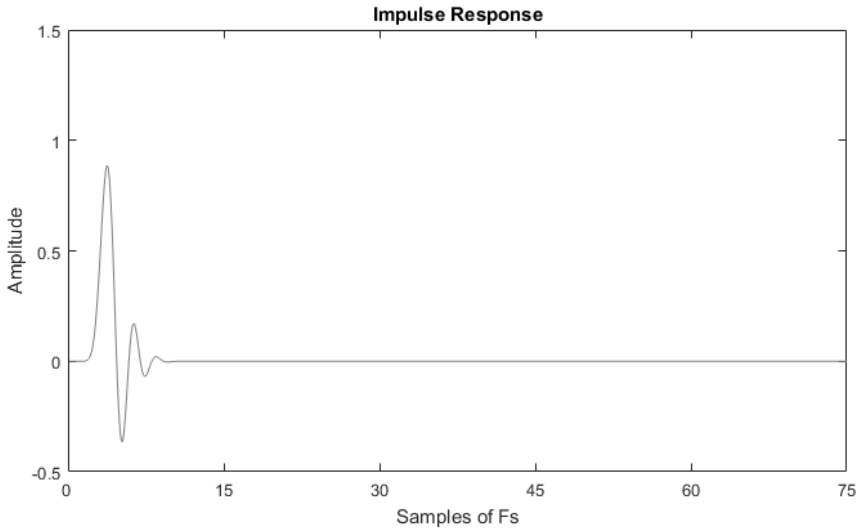
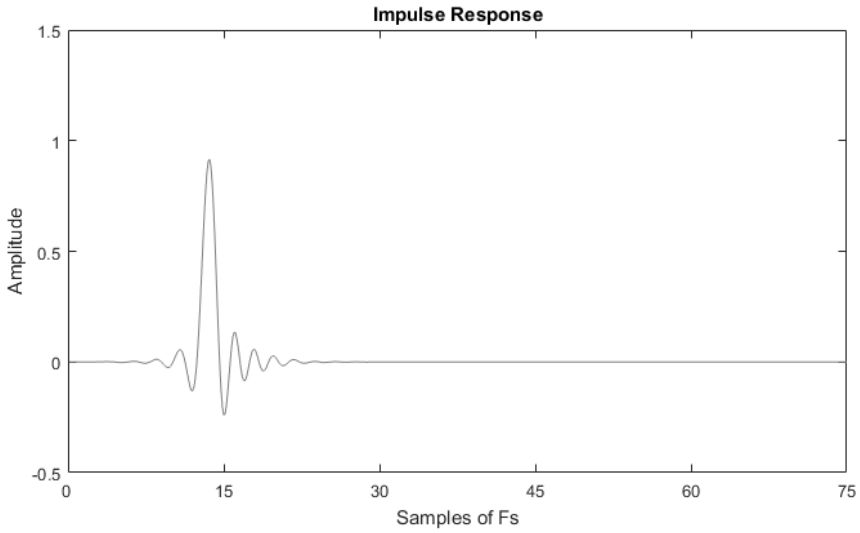
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

Table 10 - PCM Filter Impulse Response

64FS Mode

When 64FS (MCLK/FS ratio) is required, it is necessary for the ES9821 to be running in 64FS Mode. If using automatic sample rate detection with Register 0[5] AUTO_FS_DETECT, 64FS Mode cannot be automatically accessed, unless Register 0[6] AUTO_FS_DETECT_BLOCK_64FS is set to 1'b0. 64FS Mode can be manually entered by setting Register 0[4] ENABLE_64FS_MODE to 1'b1, overriding the AUTO_FS_DETECT logic.

- Register 0[6] AUTO_FS_DETECT_BLOCK_64FS
  - 1'b0: Allows AUTO_FS_DETECT to enter 64FS Mode
  - 1'b1: Blocks AUTO_FS_DETECT from entering 64FS mode (default)
- Register 0[5] AUTO_FS_DETECT
  - 1'b0: Manually set sample rate with Register 1[6:0]
  - 1'b1: Automatically determine the sample rate (default)
- Register 0[4] ENABLE_64FS_MODE
  - Use for 64FS ratios, including 705.6/768kHz sample rates

This mode enables the Minimum phase 64FS filter. See filter properties.

Note: 64FS mode is not supported in Hardware mode (HW).

Minimum phase 64FS Mode Latency

The following table shows the simulated latency at 705.6kHz sampling rate. The latency was measured at the peak amplitude of the impulse response prior to being down-sampled to 1FS. Latency delay will reduce (scale) with sampling rate.

Digital Filter	Delay(us) @ fs= 705.6 kHz
Minimum Phase 64FS	9us

Table 11 - Latency of Minimum Phase 64FS filter

Minimum Phase 64FS Filter Properties

Minimum Phase 64FS					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.57 x fs	Hz
Stop band	-94 dB	0.91 x fs			Hz
Group Delay		1.23/fs		2.68/fs	s
Flatness (ripple)	-		-		dB

Table 12 - Minimum Phase 64FS Filter Properties

Minimum Phase 64FS Filter Frequency Response

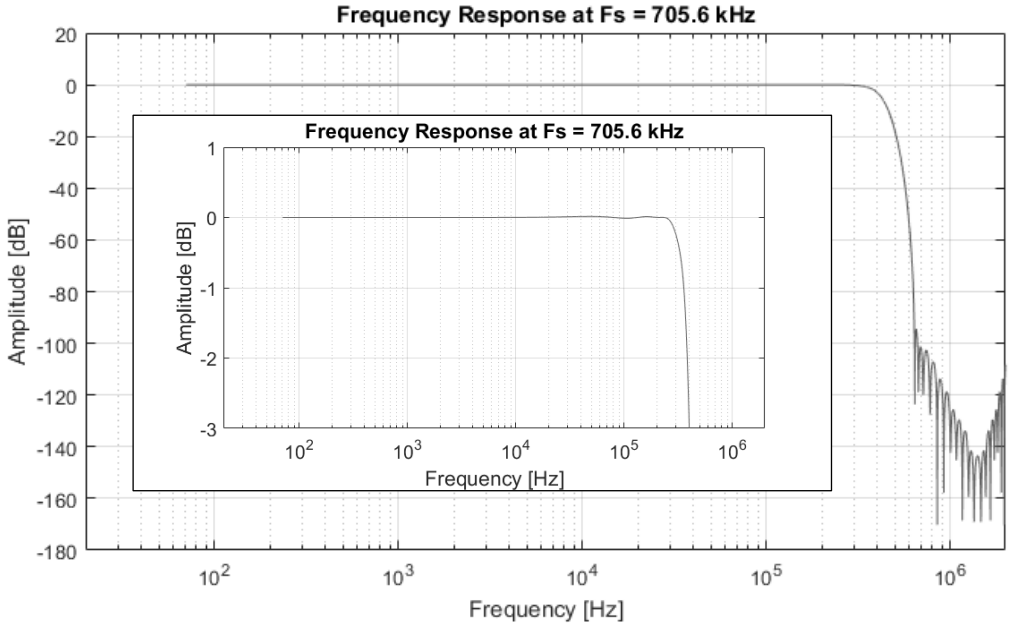


Figure 16 - Minimum Phase 64FS Filter Response

Minimum Phase 64FS Impulse Response

The following impulse responses were obtained from software simulations of these filters. The impulse responses reported below show the decimation path prior to down-sampling to 1FS and are scaled accordingly.

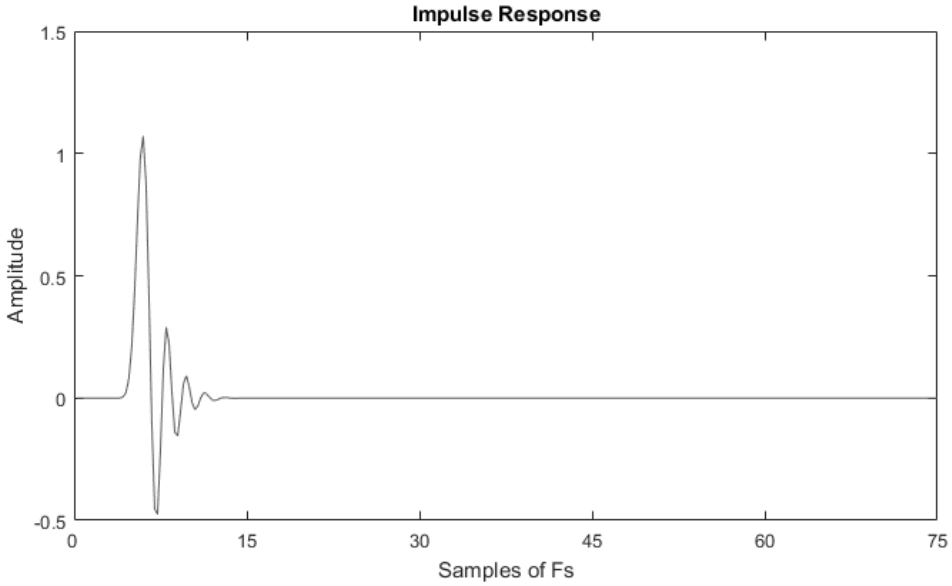


Figure 17 - Minimum Phase 64FS Impulse response

Clock Distribution

The ES9821 includes features for selecting and manipulating the input clock source.

The minimum supported external MCLK is 24.576/22.5792MHz. Below this frequency, it is required to use the APLL.

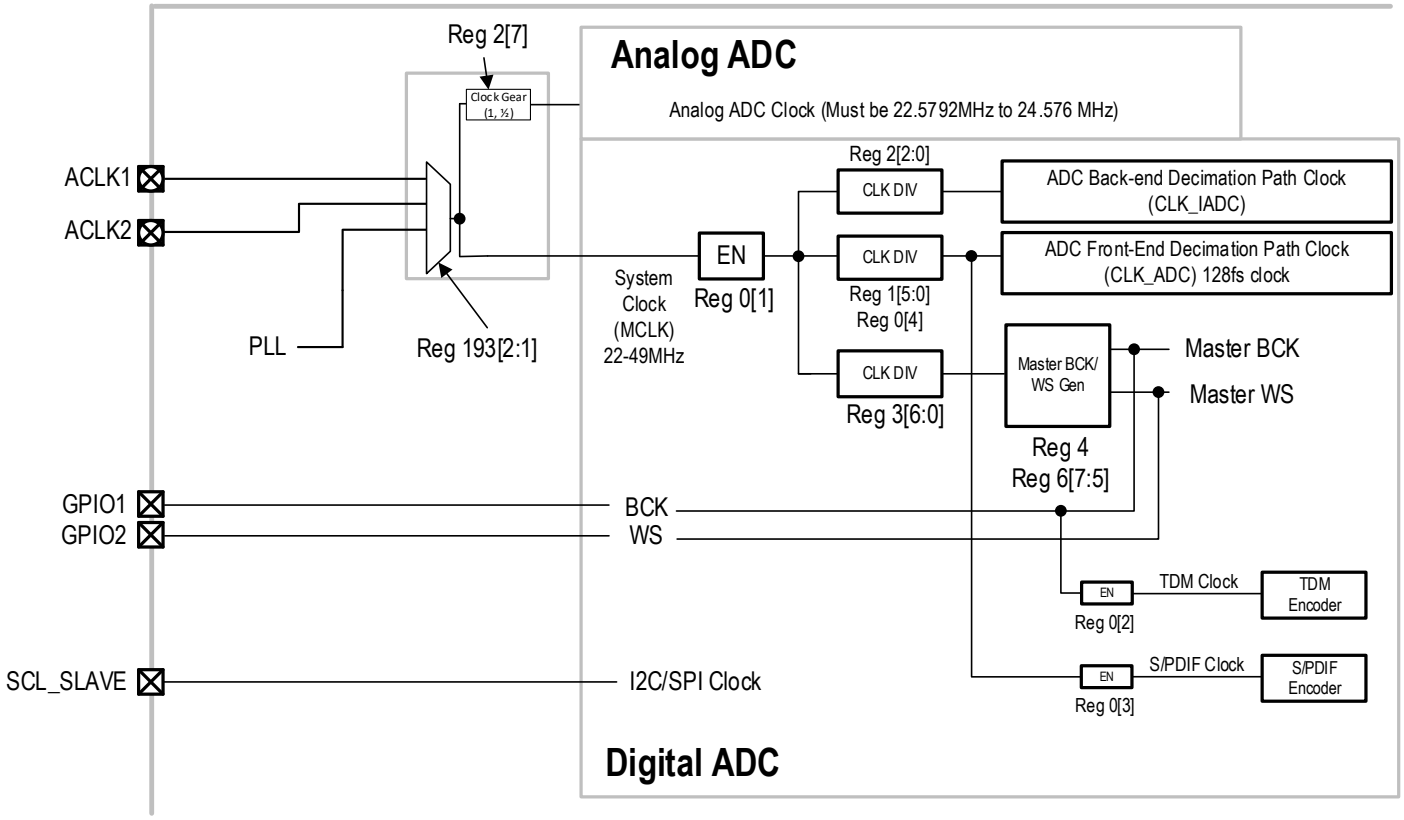


Figure 18 - ES9821 Clock Distribution

The following list shows the various clocks of the ES9821 and the associated registers for configuration.

Analog ADC Clock (ADC_CLK)

ADC_CLK must be maintained to be between 22.5792MHz & 24.576MHz

- Reg 2[7] ADC_CLK_DIV2

ADC Back-End Decimation Path Clock (CLK_IADC)

CLK_IADC must be maintained to be between 22.5792MHz & 24.576MHz

- Reg 2[2:0] SELECT_IADC_NUM

ADC Front-End Decimation Path Clock (CLK_ADC)

- Reg 0[6] AUTO_FS_DETECT_BLOCK_64FS
- Reg 0[5] AUTO_FS_DETECT
- Reg 0[4] ENABLE_64FS_MODE
- Reg 1[6] SELECT_ADC_HALF
- Reg 1[5:0] SELECT_ADC_NUM

Master BCK & WS

- Reg 1[7] AUTO_CH_DETECT
- Reg 3[7] SELECT_I²S_TDM_HALF
- Reg 3[6:0] SELECT_I²S_TDM_NUM
- Reg 4[7] MASTER_BCK_DIV1
- Reg 4[5:4] MASTER_FRAME_LENGTH
- Reg 4[3] MASTER_WS_PULSE_MODE
- Reg 4[2] MASTER_BCK_INVERT
- Reg 4[1] MASTER_WS_INVERT
- Reg 4[0] MASTER_MODE_ENABLE
- Reg 6[7:5] MASTER_WS_SCALE
- Reg 6[4:0] TDM_CH_NUM

TDM Clock (CLK_TDM_ENC)

- Reg 0[2] ENABLE_TDM_ENCODE

S/PDIF Clock (CLK_SPDIF)

- Reg 0[3] ENABLE_SPDIF_ENCODE

I²S Master Clock Rate Configurations

WS can be scaled down further than shown via Register 6 [7:5] *MASTER_WS_SCALE*.

When enabling 16-bit mode, the following registers must be modified:

- Register 63 [0:1] - enable 16-bit mode on channels 1 and 2
- Register 5 [0] - set TDM length to 16-bits
- Register 4 [5:4] - set master frame length to 16-bits

MCLK Frequency	WS [kHz]	BCK [MHz]	Bits	Ch	Register 1 [5:0] SELECT_ADC_NUM		Register 3 [6:0] SELECT_I²S_TDM_NUM	
					Value	Divider	Value	Divider
22.579 MHz	44.1	2.822	32	2	5'd3	4	7'd3	4
	88.2	5.645		2	5'd1	2	7'd1	2
	176.4	11.290		2	5'd0	1	7'd0	1
	44.1	1.411	16	2	5'd3	4	7'd3	4
	88.2	2.822		2	5'd1	2	7'd1	2
	176.4	5.645		2	5'd0	1	7'd0	1
24.576 MHz	48	3.072	32	2	5'd3	4	7'd3	4
	96	6.144		2	5'd1	2	7'd1	2
	192	12.288		2	5'd0	1	7'd0	1
	48	1.536	16	2	5'd3	4	7'd3	4
	96	3.072		2	5'd1	2	7'd1	2
	192	6.144		2	5'd0	1	7'd0	1
45.158 MHz	44.1	2.822	32	2	5'd7	8	7'd7	8
	88.2	5.645		2	5'd3	4	7'd3	4
	176.4	11.290		2	5'd1	2	7'd1	2
	352.8	22.579		2	5'd0	1	7'd0	1
	44.1	1.411	16	2	5'd7	8	7'd7	8
	88.2	2.822		2	5'd3	4	7'd3	4
	176.4	5.645		2	5'd1	2	7'd1	2
	352.8	11.290		2	5'd0	1	7'd0	1
49.152 MHz	48	3.072	32	2	5'd7	8	7'd7	8
	96	6.144		2	5'd3	4	7'd3	4
	192	12.288		2	5'd1	2	7'd1	2
	384	24.576		2	5'd0	1	7'd0	1
	48	1.536	16	2	5'd7	8	7'd7	8
	96	3.072		2	5'd3	4	7'd3	4
	192	6.144		2	5'd1	2	7'd1	2
	384	12.288		2	5'd0	1	7'd0	1

Table 13 - I²S Master Clock Rate Configurations

I²S Slave Clock Rate Configurations

MCLK Frequency	WS [kHz]	BCK	Ch	Register 1 [5:0] SELECT_ADC_NUM		Register 0 [4] ENABLE_64FS_MODE	
				Value	Divider	Value	Multiplier
22.579 MHz	44.1	512FS	2	7'd3	4	1'b0	1x
	88.2	256FS	2	7'd1	2	1'b0	1x
	176.4	128FS	2	7'd0	1	1'b0	1x
	352.8	64FS	2	7'd0	1	1'b1	2x
24.576 MHz	48	512FS	2	7'd3	4	1'b0	1x
	96	256FS	2	7'd1	2	1'b0	1x
	192	128FS	2	7'd0	1	1'b0	1x
	384	64FS	2	7'd0	1	1'b1	2x
45.158 MHz	44.1	1024FS	2	7'd7	8	1'b0	1x
	88.2	512FS	2	7'd3	4	1'b0	1x
	176.4	256FS	2	7'd1	2	1'b0	1x
	352.8	128FS	2	7'd0	1	1'b0	1x
49.152 MHz	48	1024FS	2	7'd7	8	1'b0	1x
	96	512FS	2	7'd3	4	1'b0	1x
	192	256FS	2	7'd1	2	1'b0	1x
	384	128FS	2	7'd0	1	1'b0	1x

Table 14 - I²S Slave Clock Rate Configurations

Digital Audio Output Port

Pins are configured in Master (AUX Output) or Slave (Aux Input) modes through GPIO Configurations.

PCM Pin Connections

See Audio Interface Timing (I²S) for timing criteria. Can select GPIO 4-6 for the datapath.

Pin Name	Function	Description
GPIO1/DATA_CLK	I²S BCLK	I²S Clock (Master or Slave)
GPIO2/DATA1	I²S WS	I²S WS (Master or Slave)
GPIO3/DATA2	I²S DATA	I²S DATA out (selectable for 2 channels)

Table 15 - PCM Pin Connections

TDM Pin Connections

See Registers 7-15 for configuration, Can select GPIO 4-6 for the datapath.

Pin Name	Function	Description
GPIO1/DATA_CLK	TDM BCK	TDM Clock (Master or Slave)
GPIO2/DATA1	TDM WS	TDM WS (Master or Slave)
GPIO3/DATA2	TDM DATA	TDM DATA out (default)

Table 16 - TDM Pin Connections

S/PDIF Pin Connections

S/PDIF Output is provided on GPIOs. Use GPIOx_CFG for S/PDIF output.

Pin Name	Description
GPIOx	GPIOx_CFG setting for GPIO of 4'd8 (S/PDIF output)

Table 17 - S/PDIF Pin Connections

Analog Features

APLL [4]

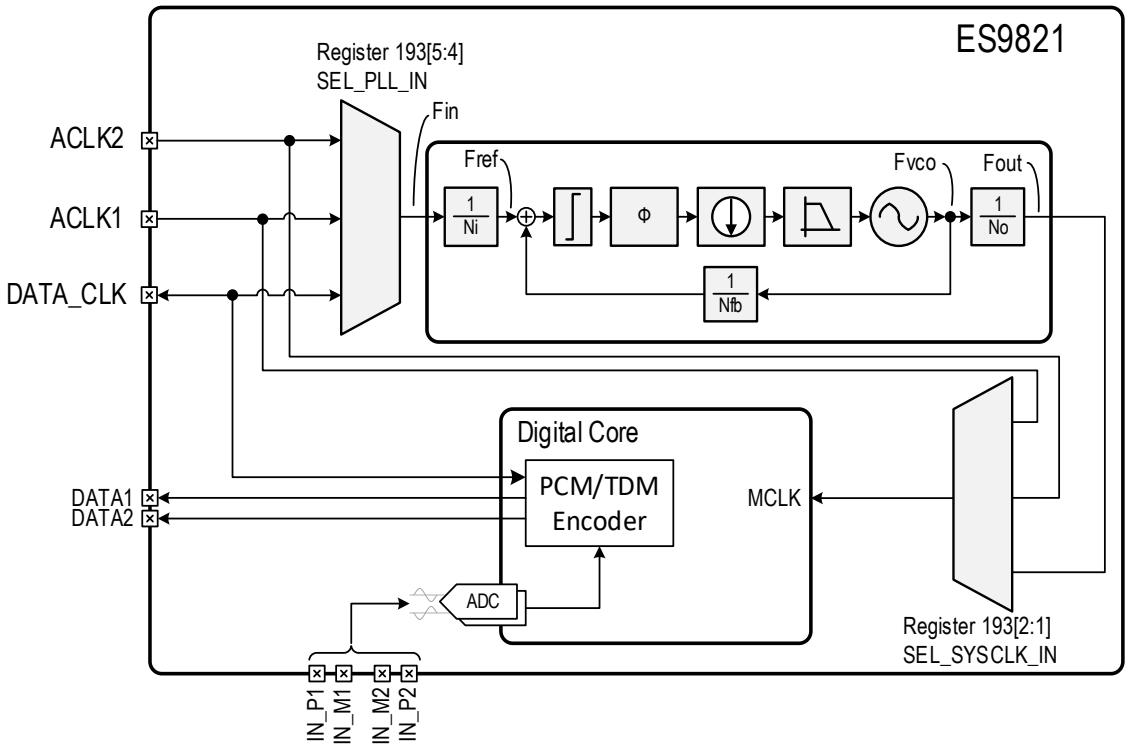


Figure 19 - Functional Block Diagram of ES9821 APLL

The ES9821 has a built in Analog PLL (APLL) for generating frequencies that are unavailable externally. For the application note on the APLL, please ask your FAE or distributor.

For calculation of the PLL frequency output, use the following formulas:

$$F_{ref} = \left(\frac{F_{in}}{N_i}\right) \qquad F_{vco} = \left(\frac{F_{in}}{N_i}\right) * N_{fb} \qquad N_{fb} = \frac{2^{25}}{FBDIV} \qquad F_{out} = \left(\frac{F_{in}}{N_i}\right) * \frac{N_{fb}}{N_o}$$

Where:

- FBDIV is a 24-bit number
- PLL frequency range requirements:
  - Fref requirement: 700kHz < Fref < 13 MHz
  - Fvco requirement: 90MHz < Fvco < 110MHz
  - Fout requirement: 22.5792/24.576MHz
- Ni = input divider
  - Accessible from Reg 202-200[9:1], **PLL_CLK_IN_DIV**
- No = output divider
  - Accessible from Reg 202-200[18:10], **PLL_CLK_OUT_DIV**
- Nfb = feedback divider
  - Accessible from Reg 199-197[23:0], **PLL_CLK_FB_DIV**

[4] Only set PLL to output 22-24MHz system clock. 45-49MHz system clock is not supported when using the PLL.

PLL Registers

- NI - Register 200-202[9:1] PLL_CLK_IN_DIV
- NO - Register 200-202[18:10] PLL_CLK_OUT_DIV
- FBDIV - Register 197-199[23:0] PLL_CLK_FB_DIV

Clock Selection

- SEL_PLL_IN - Register 193[5:4]
    - Selection of PLL clock source (ACLK1/ACLK2/BCK or DATA_CLK)
- SEL_PLL_CLKIN - Register 193[3]
    - Enables SEL_PLL_IN source input
- SEL_SYSCLK_IN - Register 193[2:1]
    - Selection of the ADC & digital core clock (ACLK1/ACLK2/PLL)

Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage • AVCC_ADC • AVCC • AVDD • DVDD (optional)	 • +3.6V with respect to Ground • +3.6V with respect to Ground • +3.6V with respect to Ground • +1.4V with respect to Ground
Storage temperature	-65°C to +150°C
Operating Junction Temperature	+125°C
Voltage range for digital input pins	-0.3V to AVDD (nom) + 0.3V
Maximum/Minimum for Input Voltage on IN_P IN_M pins	-0.4V to VREF_BUF (nom) + 1.2V
ESD Protection Human Body Model (HBM) Charge Device Model (CDM)	 2kV 500V

Table 18 - Absolute Maximum Ratings

WARNING: Stresses beyond those listed under here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

IO Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT	COMMENTS
High-level input voltage	VIH	(AVDD / 2) + 0.4		V	
Low-level input voltage	VIL		0.4	V	
High-level output voltage	VOH	AVDD - 0.2		V	IOH = ((AVDD / 2) +1.4) mA
Low-level output voltage	VOL		0.2	V	IOL = ((AVDD / 2) + 1.7) mA

Table 19 - IO Electrical Characteristics

Recommended Operating Conditions

These are the recommended operating conditions for the ES9821.

PARAMETER	SYMBOL	CONDITIONS
Operating temperature	T_A	-20°C to +85°C
AVCC		3.3V ± 5%
AVCC_ADC		3.3V ± 5%
AVDD		3.3V ± 5%
VREF		Internal 2.8V
VREF_BUF		Internal 2.8V
DVDD		Internal 1.2V
Input DC offset		AVCC/2

Table 20 - Recommended Operating Conditions

Note: The minimum supported external MCLK is 24.576/22.5792MHz. Below this frequency, it is required to use the APLL.

Recommended Power Up/Down Sequence

The recommended power up sequence for the ES9821 is shown in the figure below. All supplies and MCLK should be stable before CHIP_EN is asserted on power up. There is a delay between enabling the ADCs and a valid data output given by the below equation for t_{data_out}.

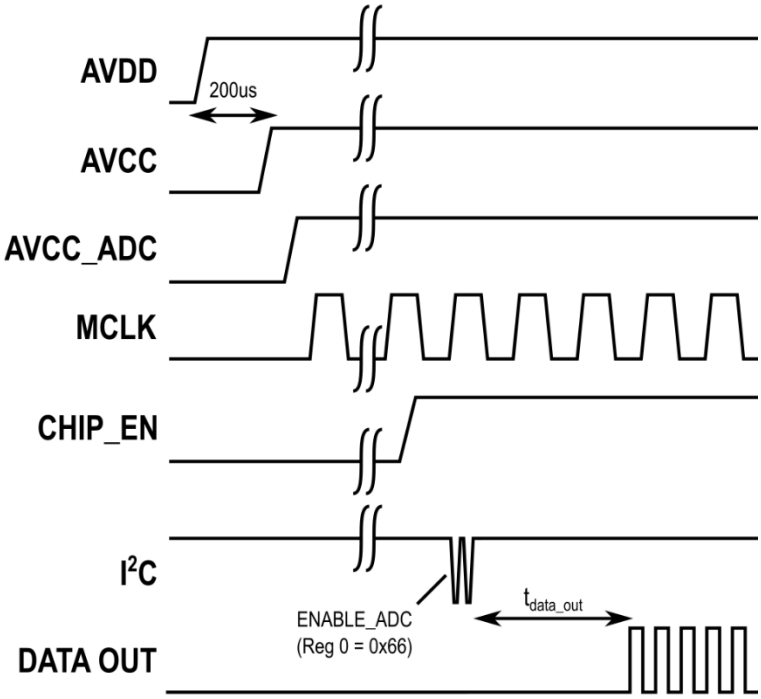


Figure 20 - Recommended Power Up Sequence

$$t_{data\_out}[s] = \left(\frac{275001}{MCLK}\right) \approx 5.6ms \ @ \ MCLK = 49.152MHz$$
$$\approx 11.2ms \ @ \ MCLK = 24.576MHz$$

The recommended power down sequence for the ES9821 is shown in the figure below.

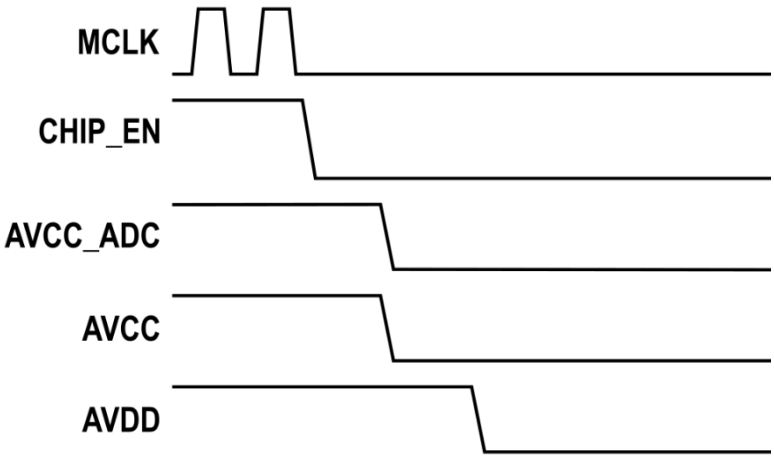


Figure 21 - Recommended Power Down Sequence

Power Consumption

Test Conditions (unless otherwise noted)

T_A = 25ºC, AVCC = AVCC_ADC = AVDD = +3.3V, fs = 48kHz, MCLK = 49.152MHz, I²S output, with -1dBFS output signal. MCLK of 49.152Mhz will work for all sample rates.

Parameter	Min	Typ.	Max	Unit
Standby, CHIP_EN = 0				
AVCC		7.1		µA
AVCC_ADC		2.2		µA
AVDD		<1		µA
48kHz, 49.152MHz, HW#3, Master Mode				
AVCC		6.5		mA
AVCC_ADC		6.7		mA
AVDD		12.1		mA
48kHz, 24.576MHz, HW#12, Slave Mode				
AVCC		6.5		mA
AVCC_ADC		6.7		mA
AVDD		7.3		mA

Table 21 - Power Consumption

Performance

Test Conditions (unless otherwise noted)

T_A = 25°C, AVCC = AVCC_ADC = AVDD = +3.3V, fs = 48kHz, MCLK = 49.152MHz, I²S output, 1kHz.

Measurements were done using ESS Evaluation Board (EVB).

Parameter			Min	Typ.	Max	Unit
Resolution				32		Bit
0dBFS Input Voltage (differential)				2		Vrms
THD+N Ratio (w/o PLL) @ fs=48kHz, BW=20Hz-20kHz	2ch mode	-1dBFS		-112	-109	dB
THD+N Ratio (w/ PLL) @ fs=48kHz, BW=20Hz-20kHz				-106	-102	
DNR A-weighted (w/o PLL)	2ch mode	-60dBFS	117	120		dB
DNR A-weighted (w/ PLL)			106	110		
Interchannel Gain Mismatch				±0.05	±0.1	dB
Input Impedance				833±15%		Ω

Table 22 - Performance

Timing Requirements

I²C Slave/Synchronous Slave Interface Timing

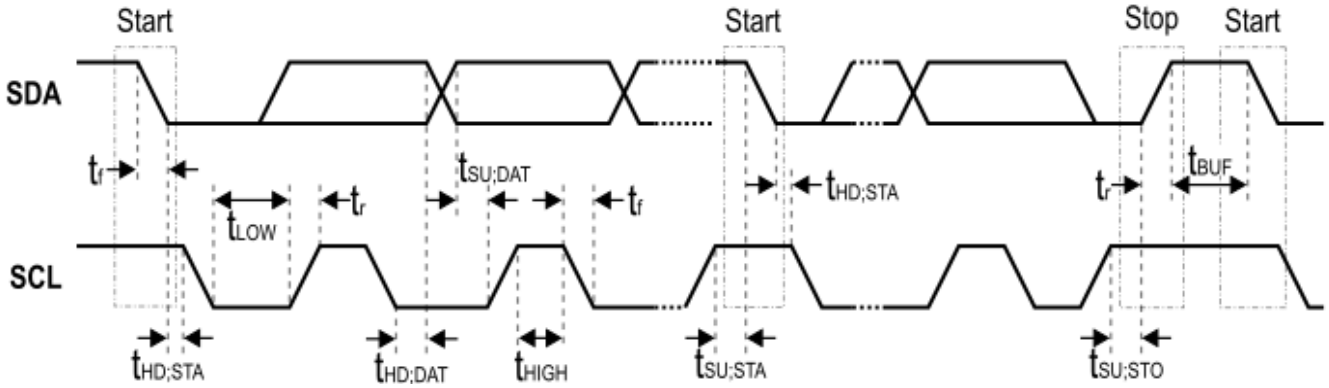


Figure 22 - I²C Slave/Synchronous Slave Control Interface Timing

Parameter	Symbol	CLK Constraint	Standard-Mode		Fast-Mode		Unit
			MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	< CLK/20	0	100	0	400	kHz
START condition hold time	$t_{HD;STA}$		4.0	-	0.6	-	µs
LOW period of SCL	t_{LOW}	>10/CLK	4.7	-	1.3	-	µs
HIGH period of SCL (>10/CLK)	t_{HIGH}	>10/CLK	4.0	-	0.6	-	µs
START condition setup time (repeat)	$t_{SU;STA}$		4.7	-	0.6	-	µs
SDA hold time from SCL falling - All except NACK read - NACK read only	$t_{HD;DAT}$		 0 2/CLK	-	 0 2/CLK	-	 µs s
SDA setup time from SCL rising	$t_{SU;DAT}$		250	-	100	-	ns
Rise time of SDA and SCL	t_r		-	1000		300	ns
Fall time of SDA and SCL	t_f		-	300		300	ns
STOP condition setup time	$t_{SU;STO}$		4	-	0.6	-	µs
Bus free time between transmissions	t_{BUF}		4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b		-	400	-	400	pF

Table 23 - I²C Slave/Synchronous Slave Control Interface Timing Definitions

PCM/TDM Timing Requirements

Master Clock (MCLK) and Bit-Clock (BCK) Timing

The ES9821 has requirements for a phase relationship requirement between MCLK (System Clock) and BCK (Bit Clock).

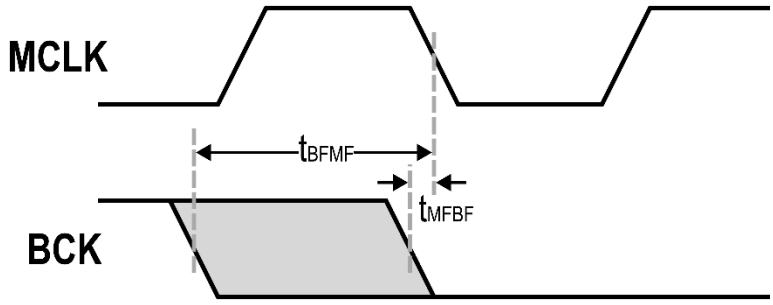


Figure 23 - 45/49MHz MCLK with BCK Phase Relationship

	Symbol	MCLK [MHz]	Minimum	Maximum	Unit
BCK "↓" to MCLK "↓"	t*BFMF*	49.152 / 45.1584	-	11	ns
MCLK "↓" to BCK "↓"	t*MFBF*		1.5	-	ns

Table 24 - Timing Relationship for 45/49MHz MCLK & BCK

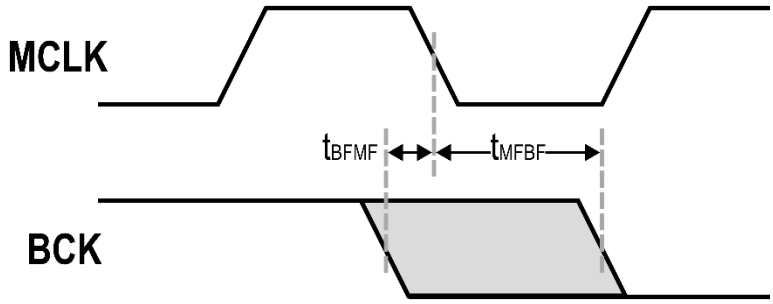


Figure 24 - 22/25MHz MCLK with BCK Phase Relationship

	Symbol	MCLK [MHz]	Minimum	Maximum	Unit
BCK "↓" to MCLK "↓"	t*BFMF*	24.576 / 22.5792	-	2	ns
MCLK "↓" to BCK "↓"	t*MFBF*	24.576 / 22.5792	-	13	ns

Table 25 - Timing Relationship for 22/24MHz MCLK & BCK

Bit-Clock (BCK) and Word-Select (WS) Timing

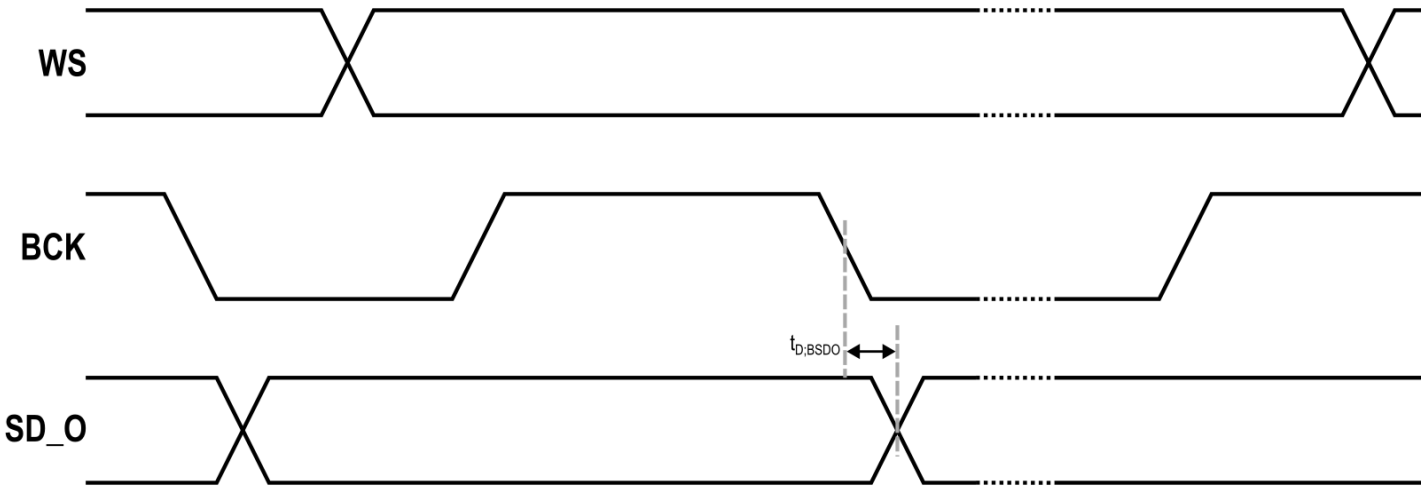


Figure 25 - Audio Interface Timing Requirements

Symbol	Min.	Typ.	Max.	Unit
$t_{D;BSDO}$	6	8	10	ns

Table 26 - Audio Interface Timing Requirements

Register Overview

ES9821 features two different register interfaces. There is a standard I²C slave interface, and a synchronous I²C slave interface. The standard I²C slave interface requires a system clock present through ACLK or from the PLL to write and read registers. The synchronous I²C slave interface does not require a system clock and allows for write-only configuration of the PLL registers to create a system clock from some reference clock (through DATA_CLK, or ACLK pins).

I²C Slave Interface (Device Address 0x40,0x42,0x44,0x46)

Read/Write Registers

Registers 0-65 (0x00 - 0x41) are read/write registers

Read-only Registers

Registers 224 - 240 (0xE0 - 0xF0) are read only registers.

I²C Synchronous Slave Interface (Device Address 0x48,0x4A,0x4C,0x4E)

This interface contains Write-only registers. These registers can be written even when there is no system clock present. When the device is inactive (CHIP_EN = 0), all peripherals are automatically disabled and all clocks are stopped.

Write-only Registers

Registers 192 - 204 (0xC0 - 0xCC) are write only registers.

Multi-Byte Registers

Multi-byte registers must be written from LSB to MSB. Data is latched when MSB is written.

Multi-byte registers must be read from LSB to MSB. Data is latched when LSB is read.

MSB is always stored in the highest register address.

Register Map

Addr (Hex)	Addr (Dec)	Register	7	6	5	4	3	2	1	0
0x00	0	SYS CONFIG	SOFT_RESET	AUTO_FS_ DETECT_ BLOCK_64FS	AUTO_FS_ DETECT	ENABLE_64FS_ MODE	ENABLE_SPDIF _ENCODE	ENABLE_TDM_ ENCODE	ENABLE_ADC	RESERVED
0x01	1	ADC CLOCK CONFIG1	AUTO_CH_ DETECT	SELECT_ADC_ HALF	SELECT_ADC_NUM					
0x02	2	ADC CLOCK CONFIG2	ADC_CLK_DIV2	RESERVED				SELECT_IADC_NUM		
0x03	3	I2S/TDM MASTER CLK CONFIG	SELECT_I2S_ TDM_HALF	SELECT_I2S_TDM_NUM						
0x04	4	I2S/TDM MASTER MODE CONFIG	MASTER_BCK_ DIV1	MASTER_WS_ IDLE	MASTER_FRAME_LENGTH		MASTER_WS_ PULSE_MODE	MASTER_BCK_ INVERT	MASTER_WS_ INVERT	MASTER_MODE _ENABLE
0x05	5	TDM CONFIG1	RESERVED					TDM_VALID_ED GE	TDM_LJ	TDM_LENGTH
0x06	6	TDM CONFIG2	MASTER_WS_SCALE			TDM_CH_NUM				
0x07	7	TDM SLOT CONFIG CH1	RESERVED		SLAVE_BCK_ INVERT	TDM_SLOT_SEL_CH1				
0x08	8	TDM SLOT CONFIG CH2	RESERVED			TDM_SLOT_SEL_CH2				
0x09-0x0B	9-11	RESERVED	RESERVED							
0x0C	12	INTERRUPT	RESERVED		INTERRUPT_ CLEAR_CH2_ PEAK_DETECT	INTERRUPT_ CLEAR_CH1_ PEAK_DETECT	RESERVED		INTERRUPT_ MASK_CH2_ PEAK_DETECT	INTERRUPT_ MASK_CH1_ PEAK_DETECT
0x0D	13	SPDIF CONFIG	SPDIF_CS							
0x0E	14		SPDIF_CS							
0x0F	15		SPDIF_CS							
0x10	16		SPDIF_CS							
0x11	17		SPDIF_CS							
0x12	18	SYNC CONTROL 1	FORCE_PLL_ LOCKED	SYNC_ POSEDGE_ FRAME	RESERVED	FORCE_FIR_ SYNC	RESERVED			
0x13	19	RESERVED	RESERVED							
0x14	20	SYNC CONTROL 2	RESERVED						AUTO_FIR_ SYNC	RESERVED
0x15-0x19	21-25	RESERVED	RESERVED							
0x1A	26	GPIO1/2 CONFIG	GPIO2_CFG				GPIO1_CFG			
0x1B	27	GPIO3/4 CONFIG	GPIO4_CFG				GPIO3_CFG			
0x1C	28	GPIO5 CONFIG	GPIO5_READ	RESERVED			GPIO5_CFG			
0x1D	29	GPIO SETTINGS 1	GPIO3_SDB	GPIO2_SDB	GPIO1_SDB	GPIO5_OE	GPIO4_OE	GPIO3_OE	GPIO2_OE	GPIO1_OE
0x1E	30	GPIO SETTINGS 2	INVERT_GPIO1	GPIO5_WK_EN	GPIO4_WK_EN	GPIO3_WK_EN	GPIO2_WK_EN	GPIO1_WK_EN	GPIO5_SDB	GPIO4_SDB
0x1F	31	GPIO SETTINGS 3	GPIO4_READ	GPIO3_READ	GPIO2_READ	GPIO1_READ	INVERT_GPIO5	INVERT_GPIO4	INVERT_GPIO3	INVERT_GPIO2
0x20	32	PWM1 COUNT	PWM1_COUNT							
0x21	33	PWM1 FREQUENCY	PWM1_FREQ							
0x22	34		PWM1_FREQ							
0x23	35	PWM2 COUNT	PWM2_COUNT							
0x24	36	PWM2 FREQUENCY	PWM2_FREQ							
0x25	37		PWM2_FREQ							
0x26	38	PWM3 COUNT	PWM3_COUNT							
0x27	39	PWM3 FREQUENCY	PWM3_FREQ							
0x28	40		PWM3_FREQ							
0x29	41	ADC DATAPATH CONTROL	RESERVED	ADC_BYPASS_ FIR2X	ADC_BYPASS_ FIR4X	RESERVED			CH1_AVR	MONO_MODE
0x2A	42	ADC DC BLOCKING & SCALE CONFIG	ADC_DATA_SCALE_CH2		ADC_DATA_SCALE_CH1		ADC_SELECT_ DC_BLOCK_ CH2	ADC_SELECT_ DC_BLOCK_ CH1	ADC_ENABLE_ DC_BLOCK_ CH2	ADC_ENABLE_ DC_BLOCK_ CH1
0x2B	43	ADC PEAK DETECTOR CONFIG	ADC_LOCK_ PEAK	ADC_DECAY_RATE					ADC_ENABLE_ PEAK_DETECT _CH2	ADC_ENABLE_ PEAK_DETECT _CH1
0x2C	44	ADC CH1 PEAK DETECTOR LEVEL	ADC_PEAK_LEVEL_CH1							
0x2D	45	ADC CH2 PEAK DETECTOR LEVEL	ADC_PEAK_LEVEL_CH2							
0x2E	46	ADC CH1 DC OFFSET	ADC_CH1_DC_OFFSET							
0x2F	47		ADC_CH1_DC_OFFSET							
0x30	48	ADC CH2 DC OFFSET	ADC_CH2_DC_OFFSET							
0x31	49		ADC_CH2_DC_OFFSET							
0x32	50	ADC CH1 VOLUME	ADC_CH1_VOLUME							
0x33	51		ADC_CH1_VOLUME							
0x34	52	ADC CH2 VOLUME	ADC_CH2_VOLUME							
0x35	53		ADC_CH2_VOLUME							
0x36	54	ADC VOLUME RATE	ADC_VOLUME_RATE							
0x37	55	THD COMP C2 CH1	THD_C2_CH1							
0x38	56		THD_C2_CH1							
0x39	57	THD COMP C3 CH1	THD_C3_CH1							
0x3A	58		THD_C3_CH1							
0x3B	59	THD COMP C2 CH2	THD_C2_CH2							
0x3C	60		THD_C2_CH2							
0x3D	61	THD COMP C3 CH2	THD_C3_CH2							
0x3E	62		THD_C3_CH2							

0x3F	63	ADC 16 BIT DEPTH	RESERVED						ENABLE_16BIT_CH2	ENABLE_16BIT_CH1
0x40	64	ADC FIR FILTER	RESERVED			ADC_FILTER_SHAPE			ENABLE_32BIT_CH2	ENABLE_32BIT_CH1
0x41	65	RESERVED	RESERVED							
0xC0	192	PLL SOFT RESET	AO_SOFT_RESET	PLL_SOFT_RESET	RESERVED					PLL_CLK_PHASE
0xC1	193	PLL CLOCK SELECT	RESERVED	EN_ADC_CLK	SEL_PLL_IN		EN_PLL_CLKIN	SEL_SYSCLK_IN		EN_SYSCLK_IN
0xC2	194	RESERVED	RESERVED							
0xC3	195	PLL VCO & CP CONFIG	PLL_CP_BIAS_SEL			RESERVED			PLL_VCO_EN	PLL_CP_EN
0xC4	196	PLL VCO CONTROL	PLL_VCO_BAND_CTRL			RESERVED				
0xC5	197	PLL FEEDBACK DIV	PLL_CLK_FB_DIV							
0xC6	198		PLL_CLK_FB_DIV							
0xC7	199		PLL_CLK_FB_DIV							
0xC8	200	PLL IN & OUT DIV	PLL_CLK_IN_DIV							PLL_FB_DIV_LOAD
0xC9	201		RESERVED		PLL_CLK_OUT_DIV				PLL_CLK_IN_DIV	
0xCA	202		PLL_REG_EN		PLL_REG_BYP		RESERVED	PLL_CLK_OUT_DIV_PHASE_ENB	RESERVED	
0xCB	203	PLL VREF SELECT	RESERVED		PLL_DIG_RSTB	RESERVED			PLL_HVREG_VREF_SEL	
0xCC	204	RESERVED	RESERVED							
0xE0	224	READ SYSTEM REGISTER 0	PEAK_FLAG_CH2	PEAK_FLAG_CH1	RESERVED			ADDR1	ADDR0	RESERVED
0xE1	225	CHIP ID	CHIP_ID							
0xE2-0xE6	226-230	RESERVED	RESERVED							
0xE7	231	TDM VALID READ	RESERVED		TDM_VALID	RESERVED				
0xE8	232	GPIO INPUT READ	RESERVED			GPIO5_I_R	GPIO4_I_R	GPIO3_I_R	GPIO2_I_R	GPIO1_I_R
0xE9-0xEC	233-236	RESERVED	RESERVED							
0xED	237	ADC PEAK CH1	ADC1_PEAK							
0xEE	238		ADC1_PEAK							
0xEF	239	ADC PEAK CH2	ADC2_PEAK							
0xF0	240		ADC2_PEAK							

Table 27 - ES9821 Register Map

Register Listing

System Registers

Register 0: SYS CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b1	1'b1	1'b0	1'b0	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RESET	Performs soft reset to digital core except for the PLL REGISTERS. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	AUTO_FS_DETECT_BLOCK_64FS	Disables AUTO_FS_DETECT from using 64FS mode. • 1'b0: AUTO_FS_DETECT can use 64FS mode • 1'b1: AUTO_FS_DETECT is unable to use 64FS mode (default)
[5]	AUTO_FS_DETECT	• 1'b0: Auto FS detect is disabled • 1'b1: Auto tune SELECT_ADC_NUM (SYS_CLK/CLK_ADC ratio) according to detected FS (default)
[4]	ENABLE_64FS_MODE	Enables 64FS mode to run the ADC decimation path at 64FS. • 1'b0: 64FS mode disabled (default) • 1'b1: 64FS mode enabled Note: This mode should be used for high sample rate (i.e., 705.6/768kHz)
[3]	ENABLE_SPDIF_ENCODE	Enables S/PDIF encoding clock. • 1'b0: S/PDIF clock disabled (default) • 1'b1: S/PDIF clock enabled
[2]	ENABLE_TDM_ENCODE	Enables I2S/TDM encoding clock. • 1'b0: I2S/TDM clock disabled • 1'b1: I2S/TDM clock enabled (default)
[1]	ENABLE_ADC	Enables ADC decimation path clocks. • 1'b0: Clocks disabled (default) • 1'b1: Clocks enabled
[0]	RESERVED	N/A

Register 1: ADC CLOCK CONFIG1

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'd3

Bits	Mnemonic	Description
[7]	AUTO_CH_DETECT	Enables BCK/FRAME ratio auto detect to determine TDM channels. • 1'b0: Disabled (default) • 1'b1: Auto detect BCK/FRAME ratio to determine the number of TDM channels
[6]	SELECT_ADC_HALF	Specifies whether to half SELECT_ADC_NUM divider. • 1'b0: Divide by SELECT_ADC_NUM + 1 (default) • 1'b1: Divide by half of SELECT_ADC_NUM + 1 Note: Can only produce half of an odd number divide
[5:0]	SELECT_ADC_NUM	Whole number divide value + 1 for CLK_ADC (SYS_CLK/divide_value). • 6'd0: Whole number divide value + 1 = 1 • 6'd3: Whole number divide value + 1 = 4 (default) • 6'd31: Whole number divide value + 1 = 32

Register 2: ADC CLOCK CONFIG2

Bits	[7]	[6:3]	[2:0]
Default	1'b0	4'b0000	3'd0

Bits	Mnemonic	Description
[7]	ADC_CLK_DIV2	Sets ADC clock rate • 1'b0: full rate (default) • 1'b1: 1/2 rate
[6:3]	RESERVED	N/A
[2:0]	SELECT_IADC_NUM	Whole number divide value + 1 for CLK_IADC (SYS_CLK/divide_value). • 3'd0: Whole number divide value + 1 = 1 (default) • 3'd1: Whole number divide value + 1 = 2 • 3'd7: Whole number divide value + 1 = 8

Register 3: I2S/TDM MASTER CLK CONFIG

Bits	[7]	[6:0]
Default	1'b0	7'd3

Bits	Mnemonic	Description
[7]	SELECT_I2S_TDM_HALF	Specifies whether to half SELECT_I2S_TDM_NUM divider. • 1'b0: Divide by SELECT_I2S_TDM_NUM + 1 (default) • 1'b1: Divide by half of SELECT_I2S_TDM_NUM + 1 Note: Can only produce half of an odd number divide
[6:0]	SELECT_I2S_TDM_NUM	Whole number divide value + 1 for I2S/TDM master encoding clock (SYS_CLK/divide_value). • 7'd0: Whole number divide value + 1 = 1 (default) • 7'd1: Whole number divide value + 1 = 2 • 7'd127: Whole number divide value + 1 = 128

Register 4: I2S/TDM MASTER MODE CONFIG

Bits	[7]	[6]	[5:4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	2'd0	1'b0	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[7]	MASTER_BCK_DIV1	When enabled, master BCK is I2S/TDM master encoding clock. Otherwise, BCK is less than or equal to (I2S/TDM master encoding clock)/2 (unless when ENABLE_64FS_MODE is set). • 1'b0: BCK is not I2S/TDM master encoding clock (default) • 1'b1: BCK is I2S/TDM master encoding clock
[6]	MASTER_WS_IDLE	Sets the value of master WS when WS is idle. • 1'b0: WS is 0 when idle (default) • 1'b1: WS is 1 when idle
[5:4]	MASTER_FRAME_LENGTH	Selects the bit length in each I2S/TDM channel in master mode. • 2'd0: 32-bit (default) • 2'd2: 16-bit • Others: Reserved
[3]	MASTER_WS_PULSE_MODE	When enabled, master WS is a pulse signal instead of a 50% duty cycle signal. The pulse width is 1 BCK cycle. • 1'b0: 50% duty cycle WS signal (default) • 1'b1: Pulse WS signal
[2]	MASTER_BCK_INVERT	Inverts master BCK. • 1'b0: Non-inverted • 1'b1: Inverted (default)
[1]	MASTER_WS_INVERT	Inverts master WS. • 1'b0: Non-inverted • 1'b1: Inverted (default)
[0]	MASTER_MODE_ENABLE	Enables I2S/TDM master mode and generates master BCK and master WS. • 1'b0: Disabled • 1'b1: Enabled (default)

Register 5: TDM CONFIG1

Bits	[7:3]	[2]	[1]	[0]
Default	5'd0	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7:3]	RESERVED	N/A
[2]	TDM_VALID_EDGE	Sets on which WS edge the frame starts. • 1'b0: Frame starts on posedge of WS • 1'b1: Frame starts on negedge of WS (default)
[1]	TDM_LJ	Sets left-justified mode. • 1'b0: Not left-justified (default) • 1'b1: Left-justified
[0]	TDM_LENGTH	Sets data length in each channel. • 1'b0: 32-bit (default) • 1'b1: 16-bit

Register 6: TDM CONFIG2

Bits	[7:5]	[4:0]
Default	3'd0	5'd1

Bits	Mnemonic	Description
[7:5]	MASTER_WS_SCALE	In I2S/TDM master mode, tunes master BCK/WS ratio by scaling master WS. It allows more TDM slots in a fixed frame. • 3'd0: No scale (default) • 3'd1: Scale down WS by 2 • 3'd2: Scale down WS by 4 • 3'd3: Scale down WS by 8 • 3'd4: Scale down WS by 16 • Others: Reserved
[4:0]	TDM_CH_NUM	Sets number of channels in each frame. • 5'd0: 1 channel • 5'd1: 2 channels (default) • 5'd31: 32 channels

Register 7: TDM SLOT CONFIG CH1

Bits	[7:6]	[5]	[4:0]
Default	2'b00	1'b0	5'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	SLAVE_BCK_INVERT	Slave BCK invert enable. • 1'b0: Non-inverted (default) • 1'b1: Invert BCK input
[4:0]	TDM_SLOT_SEL_CH1	Selects which TDM channel slot is filled by ADC Ch1 data. • 5'd0: Slot 1 (default) • 5'd1: Slot 2 • 5'd31: Slot 32

Register 8: TDM SLOT CONFIG CH2

Bits	[7:5]	[4:0]
Default	3'b000	5'd1

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	TDM_SLOT_SEL_CH2	Selects which TDM channel slot is filled by ADC Ch2 data. • 5'd0: Slot 1 • 5'd1: Slot 2 (default) • 5'd31: Slot 32

Register 11-9: RESERVED

Register 12: INTERRUPT

Bits	[7:6]	[5]	[4]	[3:2]	[1]	[0]
Default	2'b00	1'b0	1'b0	2'b00	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	INTERRUPT_CLEAR_CH2_PEAK_DETECT	Clears the peak detection interrupt of ADC Ch2 • 1'b0: Interrupt held if asserted and not masked (default) • 1'b1: Interrupt cleared
[4]	INTERRUPT_CLEAR_CH1_PEAK_DETECT	Clears the peak detection interrupt of ADC Ch1 • 1'b0: Interrupt held if asserted and not masked (default) • 1'b1: Interrupt cleared
[3:2]	RESERVED	N/A
[1]	INTERRUPT_MASK_CH2_PEAK_DETECT	Masks the peak detection interrupt of ADC Ch2 • 1'b0: Interrupt masked (default) • 1'b1: Interrupt held if asserted
[0]	INTERRUPT_MASK_CH1_PEAK_DETECT	Masks the peak detection interrupt of ADC Ch1 • 1'b0: Interrupt masked (default) • 1'b1: Interrupt held if asserted

Register 17-13: SPDIF CONFIG

Bits	[39:0]
Default	40'd0

Bits	Mnemonic	Description
[39:0]	SPDIF_CS	Configures SPDIF sub-code bits.

Register 18: SYNC CONTROL 1

Bits	[7]	[6]	[5]	[4]	[3:0]
Default	1'b1	1'b0	1'b0	1'b0	4'b0000

Bits	Mnemonic	Description
[7]	FORCE_PLL_LOCKED	Clock locking status control with PLL_LOCKED. • 1'b0: clock locking status is determined by PLL_LOCKED • 1'b1: ignores PLL_LOCKED signal from PLL and sets clock locking status to 1 (default)
[6]	SYNC_POSEDGE_FRAME	Selects which edge of the sync reference signal is used. • 1'b0: Sync to negative edge of the sync reference (default) • 1'b1: Sync to positive edge of the sync reference
[5]	RESERVED	N/A
[4]	FORCE_FIR_SYNC	Forces FIR to re-sync to the reference. • 1'b0: No force (default) • 1'b1: Forces FIR to re-sync
[3:0]	RESERVED	N/A

Register 19: RESERVED

Register 20: SYNC CONTROL 2

Bits	[7:2]	[1]	[0]
Default	6'b001111	1'b1	1'b1

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	AUTO_FIR_SYNC	Allows FIR to auto sync to the reference. • 1'b0: Auto sync disabled • 1'b1: Auto sync enabled (default)
[0]	RESERVED	N/A

Register 25-21: RESERVED

GPIO Registers

Register 26: GPIO1/2 CONFIG

Bits	[7:4]	[3:0]
Default	4'd2	4'd2

Bits	Mnemonic	Description
[7:4]	GPIO2_CFG	Configure GPIO2 GPIO Function Selection • 4'd0: Analog outputs off - shutdown • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output (default) • 4'd3: Clock valid flag - output • 4'd4: PLL locked flag - output • 4'd5: Ch1 peak interrupt - output • 4'd6: Ch2 peak interrupt - output • 4'd7: OR of all interrupts -output • 4'd8: S/PDIF data output - output • 4'd9: Output PWM1 - output • 4'd10: Output PWM2 - output • 4'd11: Output PWM3 - output • 4'd12: Reserved • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output
[3:0]	GPIO1_CFG	Configure GPIO1 GPIO Function Selection • 4'd0: Analog outputs off - shutdown • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output (default) • 4'd3: Clock valid flag - output • 4'd4: PLL locked flag - output • 4'd5: Ch1 peak interrupt - output • 4'd6: Ch2 peak interrupt - output • 4'd7: OR of all interrupts -output • 4'd8: S/PDIF data output - output • 4'd9: Output PWM1 - output • 4'd10: Output PWM2 - output • 4'd11: Output PWM3 - output • 4'd12: Reserved • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output

Register 27: GPIO3/4 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd2

Bits	Mnemonic	Description
[7:4]	GPIO4_CFG	Configure GPIO4 GPIO Function Selection • 4'd0: Analog outputs off - shutdown • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output • 4'd3: Clock valid flag - output • 4'd4: PLL locked flag - output • 4'd5: Ch1 peak interrupt - output • 4'd6: Ch2 peak interrupt - output • 4'd7: OR of all interrupts -output • 4'd8: S/PDIF data output - output • 4'd9: Output PWM1 - output • 4'd10: Output PWM2 - output • 4'd11: Output PWM3 - output • 4'd12: Reserved • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output
[3:0]	GPIO3_CFG	Configure GPIO3 GPIO Function Selection • 4'd0: Analog outputs off - shutdown • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output (default) • 4'd3: Clock valid flag - output • 4'd4: PLL locked flag - output • 4'd5: Ch1 peak interrupt - output • 4'd6: Ch2 peak interrupt - output • 4'd7: OR of all interrupts -output • 4'd8: S/PDIF data output - output • 4'd9: Output PWM1 - output • 4'd10: Output PWM2 - output • 4'd11: Output PWM3 - output • 4'd12: Reserved • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output

Register 28: GPIO5 CONFIG

Bits	[7]	[6:4]	[3:0]
Default	1'b0	3'd0	4'd0

Bits	Mnemonic	Description
[7]	GPIO5_READ	GPIO5 readback enable. • 1'b0: GPIO5 readback disabled (default) • 1'b1: Allows readback of GPIO5 input
[6:4]	RESERVED	N/A
[3:0]	GPIO5_CFG	Configure GPIO5 GPIO Function Selection • 4'd0: Analog outputs off - shutdown • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output • 4'd3: Clock valid flag - output • 4'd4: PLL locked flag - output • 4'd5: Ch1 peak interrupt - output • 4'd6: Ch2 peak interrupt - output • 4'd7: OR of all interrupts -output • 4'd8: S/PDIF data output - output • 4'd9: Output PWM1 - output • 4'd10: Output PWM2 - output • 4'd11: Output PWM3 - output • 4'd12: Reserved • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output

Register 29: GPIO SETTINGS 1

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b1	1'b1	1'b0	1'b0	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[7]	GPIO3_SDB	GPIO3 input enable. • 1'b0: GPIO3 input disabled (default) • 1'b1: GPIO3 input enabled
[6]	GPIO2_SDB	GPIO2 input enable. • 1'b0: GPIO2 input disabled • 1'b1: GPIO2 input enabled (default)
[5]	GPIO1_SDB	GPIO1 input enable. • 1'b0: GPIO1 input disabled • 1'b1: GPIO1 input enabled (default)
[4]	GPIO5_OE	GPIO5 output enable. • 1'b0: Tristate GPIO5 output (default) • 1'b1: GPIO5 output enabled
[3]	GPIO4_OE	GPIO4 output enable. • 1'b0: Tristate GPIO4 output (default) • 1'b1: GPIO4 output enabled
[2]	GPIO3_OE	GPIO3 output enable. • 1'b0: Tristate GPIO3 output • 1'b1: GPIO3 output enabled (default)
[1]	GPIO2_OE	GPIO2 output enable. • 1'b0: Tristate GPIO2 output • 1'b1: GPIO2 output enabled (default)
[0]	GPIO1_OE	GPIO1 output enable. • 1'b0: Tristate GPIO1 output • 1'b1: GPIO1 output enabled(default)

Register 30: GPIO SETTINGS 2

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	INVERT_GPIO1	GPIO1 invert enable. • 1'b0: Non-invert (default) • 1'b1: Invert GPIO1 output
[6]	GPIO5_WK_EN	GPIO5 weak keeper enable. • 1'b0: GPIO5 weak keeper disabled (default) • 1'b1: GPIO5 weak keeper enabled
[5]	GPIO4_WK_EN	GPIO4 weak keeper enable. • 1'b0: GPIO4 weak keeper disabled (default) • 1'b1: GPIO4 weak keeper enabled
[4]	GPIO3_WK_EN	GPIO3 weak keeper enable. • 1'b0: GPIO3 weak keeper disabled (default) • 1'b1: GPIO3 weak keeper enabled
[3]	GPIO2_WK_EN	GPIO2 weak keeper enable. • 1'b0: GPIO2 weak keeper disabled (default) • 1'b1: GPIO2 weak keeper enabled
[2]	GPIO1_WK_EN	GPIO1 weak keeper enable. • 1'b0: GPIO1 weak keeper disabled (default) • 1'b1: GPIO1 weak keeper enabled
[1]	GPIO5_SDB	GPIO5 input enable. • 1'b0: GPIO5 input disabled (default) • 1'b1: GPIO5 input enabled
[0]	GPIO4_SDB	GPIO4 input enable. • 1'b0: GPIO4 input disabled (default) • 1'b1: GPIO4 input enabled

Register 31: GPIO SETTINGS 3

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	GPIO4_READ	GPIO 4 readback enable. • 1'b0: GPIO4 readback disabled (default) • 1'b1: Allows readback of GPIO4 input
[6]	GPIO3_READ	GPIO 3 readback enable. • 1'b0: GPIO3 readback disabled (default) • 1'b1: Allows readback of GPIO3 input
[5]	GPIO2_READ	GPIO 2 readback enable. • 1'b0: GPIO2 readback disabled (default) • 1'b1: Allows readback of GPIO2 input
[4]	GPIO1_READ	GPIO 1 readback enable. • 1'b0: GPIO1 readback disabled (default) • 1'b1: Allows readback of GPIO1 input
[3]	INVERT_GPIO5	GPIO5 invert enable. • 1'b0: Non-invert (default) • 1'b1: Invert GPIO5 output
[2]	INVERT_GPIO4	GPIO4 invert enable. • 1'b0: Non-invert (default) • 1'b1: Invert GPIO4 output
[1]	INVERT_GPIO3	GPIO3 invert enable. • 1'b0: Non-invert (default) • 1'b1: Invert GPIO3 output
[0]	INVERT_GPIO2	GPIO2 invert enable. • 1'b0: Non-invert (default) • 1'b1: Invert GPIO2 output

Register 32: PWM1 COUNT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	PWM1_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 34-33: PWM1 FREQUENCY

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	PWM1_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $$\text{frequency [Hz]} = \frac{\text{SYS\_CLK}}{\text{PWM1\_FREQ} + 1}$$ $$\text{Duty Cycle [\%]} = \left(\frac{\text{PWM1\_COUNT}}{\text{PWM1\_FREQ} + 1}\right) \cdot 100$$

Register 35: PWM2 COUNT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	PWM2_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 37-36: PWM2 FREQUENCY

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	PWM2_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $$\text{frequency [Hz]} = \frac{\text{SYS\_CLK}}{\text{PWM2\_FREQ} + 1}$$ $$\text{Duty Cycle [\%]} = \left(\frac{\text{PWM2\_COUNT}}{\text{PWM2\_FREQ} + 1}\right) \cdot 100$$

Register 38: PWM3 COUNT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	PWM3_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 40-39: PWM3 FREQUENCY

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	PWM3_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $$\text{frequency [Hz]} = \frac{\text{SYS\_CLK}}{\text{PWM3\_FREQ} + 1}$$ $$\text{Duty Cycle [\%]} = \left(\frac{\text{PWM3\_COUNT}}{\text{PWM3\_FREQ} + 1}\right) \cdot 100$$

ADC Registers

Register 41: ADC DATAPATH CONTROL

Bits	[7]	[6]	[5]	[4:2]	[1]	[0]
Default	1'b1	1'b0	1'b0	3'b000	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	ADC_BYPASS_FIR2X	DFir_2x bypass control. • 1'b0: Non-bypass (default) • 1'b1: Bypass DFir_2x
[5]	ADC_BYPASS_FIR4X	DFir_4x bypass control. • 1'b0: Non-bypass (default) • 1'b1: Bypass DFir_4x
[4:2]	RESERVED	N/A
[1]	CH1_AVR	Use (CH1+CH2)/2 as CH1 data. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	MONO_MODE	Mute CH2 decimation path. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 42: ADC DC BLOCKING & SCALE CONFIG

Bits	[7:6]	[5:4]	[3]	[2]	[1]	[0]
Default	2'd0	2'd0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	ADC_DATA_SCALE_CH2	ADC CH2 data scale. • 2'd0: +0dB • 2'd1: +6dB • 2'd2: +12dB • 2'd3: +18dB
[5:4]	ADC_DATA_SCALE_CH1	ADC CH1 data scale. • 2'd0: +0dB • 2'd1: +6dB • 2'd2: +12dB • 2'd3: +18dB
[3]	ADC_SELECT_DC_BLOCK_CH2	Controls DC blocking filter output for CH2 output. • 1'b0: Bypass DC blocking filter output (default) • 1'b1: Use DC blocking filter output
[2]	ADC_SELECT_DC_BLOCK_CH1	Controls DC blocking filter output for CH1 output. • 1'b0: Bypass DC blocking filter output (default) • 1'b1: Use DC blocking filter output
[1]	ADC_ENABLE_DC_BLOCK_CH2	CH2 DC blocking filter control. • 1'b0: Disabled (default) • 1'b1: Enable DC blocking filter
[0]	ADC_ENABLE_DC_BLOCK_CH1	CH1 DC blocking filter control. • 1'b0: Disabled (default) • 1'b1: Enable DC blocking filter

Register 43: ADC PEAK DETECTOR CONFIG

Bits	[7]	[6:2]	[1]	[0]
Default	1'b0	5'd10	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ADC_LOCK_PEAK	Locks the stored value of the peak detectors (CH1/2) for reading back. • 1'b0: Stored value is allowed to update (default) • 1'b1: Stored value is locked
[6:2]	ADC_DECAY_RATE	Sets the speed at which the stored value of the peak detector will decay when the input signal is below the stored value. • 5'd0: Instant decay • 5'd10: Default • 5'd31: Slowest decay
[1]	ADC_ENABLE_PEAK_DETECT_CH2	Enables the ADC CH2 signal peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ADC_ENABLE_PEAK_DETECT_CH1	Enables the ADC CH1 signal peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 44: ADC CH1 PEAK DETECTOR LEVEL

Bits	[7:0]
Default	8'hFF

Bits	Mnemonic	Description
[7:0]	ADC_PEAK_LEVEL_CH1	Threshold value of the CH1 peak detector. • 8'h01: -48dB • 8'hFF: 0dB (default)

Register 45: ADC CH2 PEAK DETECTOR LEVEL

Bits	[7:0]
Default	8'hFF

Bits	Mnemonic	Description
[7:0]	ADC_PEAK_LEVEL_CH2	Threshold value of the CH2 peak detector. • 8'h01: -48dB • 8'hFF: 0dB (default)

Register 47-46: ADC CH1 DC OFFSET

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	ADC_CH1_DC_OFFSET	ADC CH1 signed DC offset. • Negative offset is valid from 16'h8000 (-30dB) to 16'hFFFF (-114dB). • 16'h0000: Zero offset (default) • Positive offset is valid from 16'h7FFF (-30dB) to 16'h0001 (-114dB). $\text{dc\_offset [dB]} = 20 \cdot \log10\left(\frac{\lvert\text{ADC\_CH1\_DC\_OFFSET}\rvert}{(2^{15}-1)\cdot 2^{5}}\right)$

Register 49-48: ADC CH2 DC OFFSET

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	ADC_CH2_DC_OFFSET	ADC CH2 signed DC offset. • Negative offset is valid from 16'h8000 (-30dB) to 16'hFFFF (-114dB). • 16'h0000: Zero offset (default) • Positive offset is valid from 16'h7FFF (-30dB) to 16'h0001 (-114dB). $\text{dc\_offset [dB]} = 20 \cdot \log10\left(\frac{\lvert\text{ADC\_CH2\_DC\_OFFSET}\rvert}{(2^{15}-1)\cdot 2^{5}}\right)$

Register 51-50: ADC CH1 VOLUME

Bits	[15:0]
Default	16'h7FFF

Bits	Mnemonic	Description
[15:0]	ADC_CH1_VOLUME	Next desired ADC CH1 signed volume coefficient. • 16'h0000: Mute • 16'h0001 (-90dB): Minimum • 16'h7FFF (0dB): Maximum (default) Note: 16'h8000 to 16'hFFFF is a phase inverted version of the volume. $\text{volume [dB]} = 20 \cdot \log10\left(\frac{\lvert\text{ADC\_CH1\_VOLUME}\rvert}{2^{15}-1}\right)$

Register 53-52: ADC CH2 VOLUME

Bits	[15:0]
Default	16'h7FFF

Bits	Mnemonic	Description
[15:0]	ADC_CH2_VOLUME	Next desired ADC CH2 signed volume coefficient. • 16'h0000: Mute • 16'h0001 (-90dB): Minimum • 16'h7FFF (0dB): Maximum (default) Note: 16'h8000 to 16'hFFFF is a phase inverted version of the volume. $\text{volume [dB]} = 20 \cdot \log10\left(\frac{\lvert\text{ADC\_CH2\_VOLUME}\rvert}{2^{15}-1}\right)$

Register 54: ADC VOLUME RATE

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	ADC_VOLUME_RATE	Value by which the old coefficient value is incremented/decremented to reach the new coefficient. • 8'h00: Instant (default) • 8'h01: Slowest ramp rate • 8'hFF: Fastest ramp rate

Register 56-55: THD COMP C2 CH1

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	THD_C2_CH1	A 16-bit signed coefficient for correcting for the CH1 second harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$

Register 58-57: THD COMP C3 CH1

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	THD_C3_CH1	A 16-bit signed coefficient for correcting for the CH1 third harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$

Register 60-59: THD COMP C2 CH2

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	THD_C2_CH2	A 16-bit signed coefficient for correcting for the CH2 second harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$

Register 62-61: THD COMP C3 CH2

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	THD_C3_CH2	A 16-bit signed coefficient for correcting for the CH2 third harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$

Register 63: ADC 16 BIT DEPTH

Bits	[7:2]	[1]	[0]
Default	6'b100100	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	ENABLE_16BIT_CH2	Sets CH2 output bit depth. • 1'b0: CH2 decimation path output is 24-bit (default) • 1'b1: CH2 decimation path output is 16-bit
[0]	ENABLE_16BIT_CH1	Sets CH1 output bit depth. • 1'b0: CH1 decimation path output is 24-bit (default) • 1'b1: CH1 decimation path output is 16-bit

Register 64: ADC FIR FILTER

Bits	[7:5]	[4:2]	[1]	[0]
Default	3'd4	3'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:2]	ADC_FILTER_SHAPE	Selects the 8x decimation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase fast roll-off apodizing • 3'd2: Linear phase fast roll-off • 3'd3: Linear phase fast roll-off low ripple • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion
[1]	ENABLE_32BIT_CH2	32-bit CH2 data output enable. ENABLE_16BIT_CH2 has priority of ENABLE_32BIT_CH2. • 1'b0: CH2 output is 24-bit (default) • 1'b1: CH2 output is 32-bit Note: Requires ADC_ENABLE_DC_BLOCK_CH2 to be set.
[0]	ENABLE_32BIT_CH1	32-bit CH1 data output enable. ENABLE_16BIT_CH1 has priority of ENABLE_32BIT_CH1. • 1'b0: CH1 ouput is 24-bit (default) • 1'b1: CH1 output is 32-bit Note: Requires ADC_ENABLE_DC_BLOCK_CH1 to be set.

Register 65: RESERVED

PLL Registers

Register 192: PLL SOFT RESET

Bits	[7]	[6]	[5:1]	[0]
Default	1'b0	1'b0	5'b00000	1'b0

Bits	Mnemonic	Description
[7]	AO_SOFT_RESET	Performs soft reset to the digital core and clocked registers (0-64). • 1'b0: Disabled (default) • 1'b1: Enable
[6]	PLL_SOFT_RESET	Performs soft reset to only the Always-On Registers (192-203). • 1'b0: Disabled (default) • 1'b1: Enable
[5:1]	RESERVED	N/A
[0]	PLL_CLK_PHASE	Digital/analog ADC clock invert phase enable. • 1'b0: Digital/analog ADC clocks have inverted phase (default) • 1'b1: Digital/analog ADC clocks have the same phase (recommended value)

Register 193: PLL CLOCK SELECT

Bits	[7]	[6]	[5:4]	[3]	[2:1]	[0]
Default	1'b0	1'b1	2'b10	1'b0	2'b00	1'b1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	EN_ADC_CLK	Enables analog ADC clock. • 1'b0: Disabled • 1'b1: Enabled (default)
[5:4]	SEL_PLL_IN	Selects PLL input clock source when EN_PLL_CLKIN is set. • 2'b00: ACLK1 • 2'b01: ACLK2 • 2'b10: DATA_CLK (default) • 2'b11: Reserved
[3]	EN_PLL_CLKIN	Allows SEL_PLL_IN to select PLL input clocks. • 1'b0: Disables SEL_PLL_IN (default) • 1'b1: Enables SEL_PLL_IN
[2:1]	SEL_SYSCLK_IN	Selects digital core and ADC clock source when EN_ANA_CLKIN is set. • 2'b00: ACLK1 (default) • 2'b01: ACLK2 • 2'b10: PLL • 2'b11: Reserved
[0]	EN_SYSCLK_IN	Enables clock outputs to the digital core. • 1'b0: Disabled • 1'b1: Enabled (default)

Register 194: RESERVED

Register 195: PLL VCO & CP CONFIG

Bits	[7:5]	[4:2]	[1]	[0]
Default	3'b111	3'b111	1'b0	1'b0

Bits	Mnemonic	Description
[7:5]	PLL_CP_BIAS_SEL	Sets the Charge Pump current: • 3'b011: 4uA (recommended value) • 3'b111: 8uA (default)
[4:2]	RESERVED	N/A
[1]	PLL_VCO_EN	Enables/disables the PLL voltage-controlled oscillator (VCO). • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	PLL_CP_EN	Enables/disables the PLL charge pump. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 196: PLL VCO CONTROL

Bits	[7:5]	[4:0]
Default	3'b011	5'b00011

Bits	Mnemonic	Description
[7:5]	PLL_VCO_BAND_CTRL	Selects the frequency band of the VCO. • 3'b010: (recommended value) • 3'b011: (default)
[4:0]	RESERVED	N/A

Register 199-197: PLL FEEDBACK DIV

Bits	[23:0]
Default	24'd0

Bits	Mnemonic	Description
[23:0]	PLL_CLK_FB_DIV	Sets the PLL clock feedback divider. • 24'd0: Reserved (default) • 24'dn: Divide by 2^25/n

Register 202-200: PLL IN & OUT DIV

Bits	[23:22]	[21:20]	[19]	[18]	[17:14]	[13:10]	[9:1]	[0]
Default	2'b00	2'b00	1'b1	1'b0	4'd0	4'd0	9'd0	1'b0

Bits	Mnemonic	Description
[23:22]	PLL_REG_EN	Enables/disables the PLL regulators. • 2'b00: Disables the PLL regulators • 2'b11: Enables the PLL regulators (Normal Operation) Note: Other options not valid
[21:20]	PLL_REG_BYP	Bypass mode of the PLL regulators. • 2'b00: Normal Operation • 2'b11: Bypass the PLL regulators Note: Other options not valid
[19]	RESERVED	N/A
[18]	PLL_CLK_OUT_DIV_PHASE_ENB	• 1'b0: Locks the PLL clock output divider phase. (default) • 1'b1: Disabled
[17:14]	RESERVED	N/A
[13:10]	PLL_CLK_OUT_DIV	Sets the Output Division (No) of the PLL. • 4'd0: Divide by 1 • 4'd1: Divide by 2 (Normal starting value) • 4'd3: Divide by 4 • 4'dn: Divide by (n + 1)
[9:1]	PLL_CLK_IN_DIV	Sets the Input Division (Ni) of the PLL. • 9'd0: Divide by 1 • 9'd1: Divide by 2 (Normal starting value) • 9'd3: Divide by 4 • 9'dn: Divide by (n + 1)
[0]	PLL_FB_DIV_LOAD	Load PLL_CLK_FB_DIV • Write 1'b1 then 1'b0 to load PLL_CLK_FB_DIV value

Register 203: PLL VREF SELECT

Bits	[7:6]	[5]	[4:2]	[1:0]
Default	2'b00	1'b0	3'b010	2'b01

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	PLL_DIG_RSTB	Resets the Digital core of the PLL.
[4:2]	RESERVED	N/A
[1:0]	PLL_HVREG_VREF_SEL	PLL HVREG reference voltage selection • 2'b00: 1.6V (optimum value) • 2'b01: 1.7V (default)

Register 204: RESERVED

Readback Registers

Register 224: READ SYSTEM REGISTER 0

Bits	[7]	[6]	[5:3]	[2]	[1]	[0]
Default	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	PEAK_FLAG_CH2	ADC CH2 peak detection interrupt readback. • 1'b0: Inactive • 1'b1: Active
[6]	PEAK_FLAG_CH1	ADC CH1 peak detection interrupt readback. • 1'b0: Inactive • 1'b1: Active
[5:3]	RESERVED	N/A
[2]	ADDR1	Readback of the ADDR1 pin.
[1]	ADDR0	Readback of the ADDR0 pin.
[0]	RESERVED	N/A

Register 225: CHIP ID

Bits	[7:0]
Default	8'h88

Bits	Mnemonic	Description
[7:0]	CHIP_ID	ES9821: 0x88

Register 230-226: RESERVED

Register 231: TDM VALID READ

Bits	[7:6]	[5]	[4:0]
Default	-	-	-

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	TDM_VALID	TDM valid flag
[4:0]	RESERVED	N/A

Register 232: GPIO INPUT READ

Bits	[7:5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4]	GPIO5_I_R	GPIO5 input readback.
[3]	GPIO4_I_R	GPIO4 input readback.
[2]	GPIO3_I_R	GPIO3 input readback.
[1]	GPIO2_I_R	GPIO2 input readback.
[0]	GPIO1_I_R	GPIO1 input readback.

Register 236-233: RESERVED

Register 238-237: ADC PEAK CH1

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	ADC1_PEAK	Ch1 detected signal peak value readback. Note: Requires reg43[0] ADC_ENABLE_PEAK_DETECT_CH1 to enable functionality. $\text{Peak [dB]} = 20 \cdot \log10\left(\frac{\text{PEAK\_LEVEL\_CH1}}{2^{16}-1}\right) + 1$

Register 240-239: ADC PEAK CH2

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	ADC2_PEAK	Ch2 detected signal peak value readback. Note: Requires reg43[1] ADC_ENABLE_PEAK_DETECT_CH2 to enable functionality. $\text{Peak [dB]} = 20 \cdot \log10\left(\frac{\text{PEAK\_LEVEL\_CH2}}{2^{16}-1}\right) + 1$

ES9821 Reference Schematic (Hardware Mode)[5]

See Hardware section for additional details on configuration for Hardware mode.

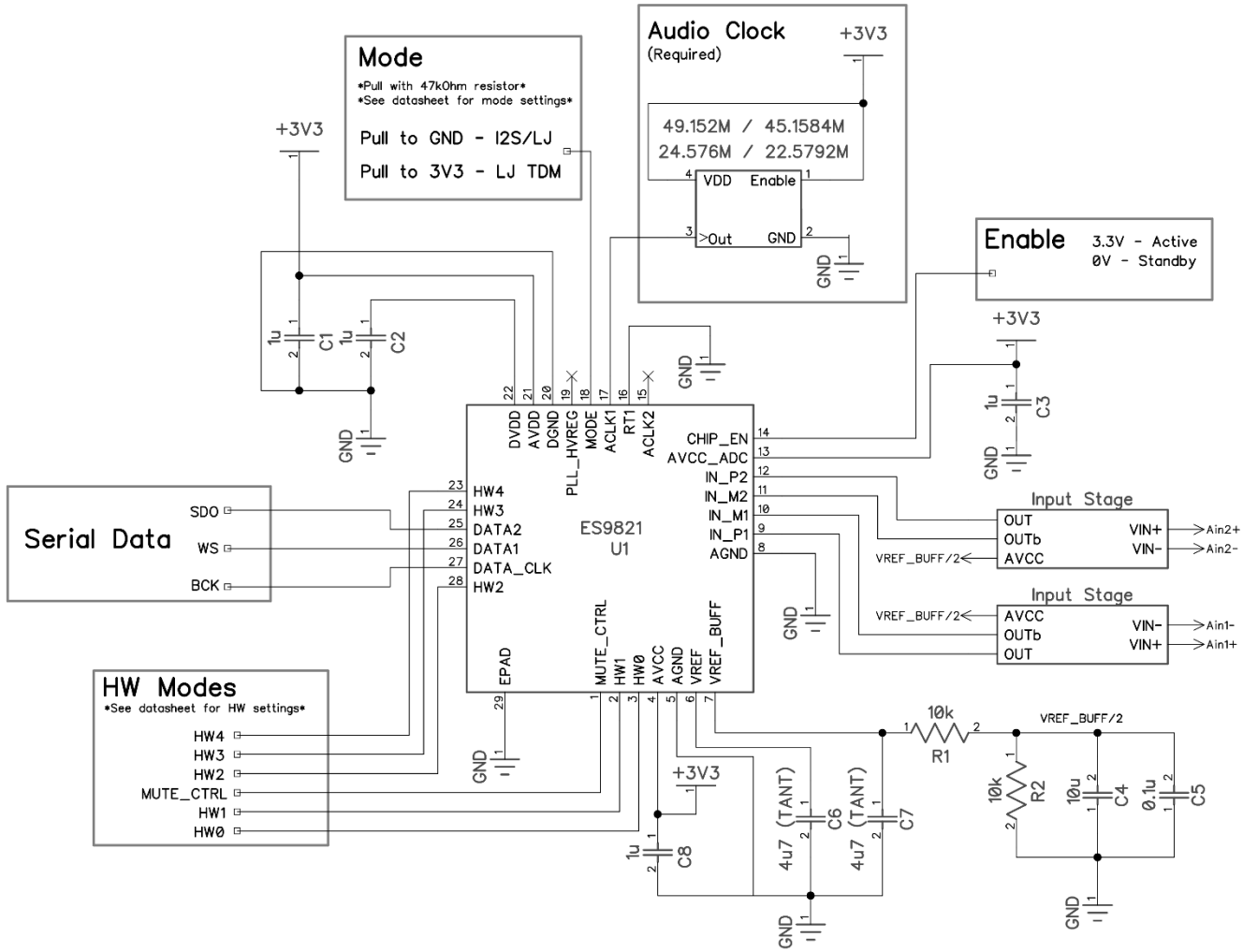


Figure 26 - ES9821Q Reference Schematic for Normal Operation in Hardware (HW) Mode

Schematic subject to change

Note: It is recommended to use Tantalum capacitors (where indicated) to achieve the highest performance

[5] Pin 29 QFN Package Pad (EPAD) should be connected to DGND.

ES9821 Reference Schematic (Software Mode)[6]

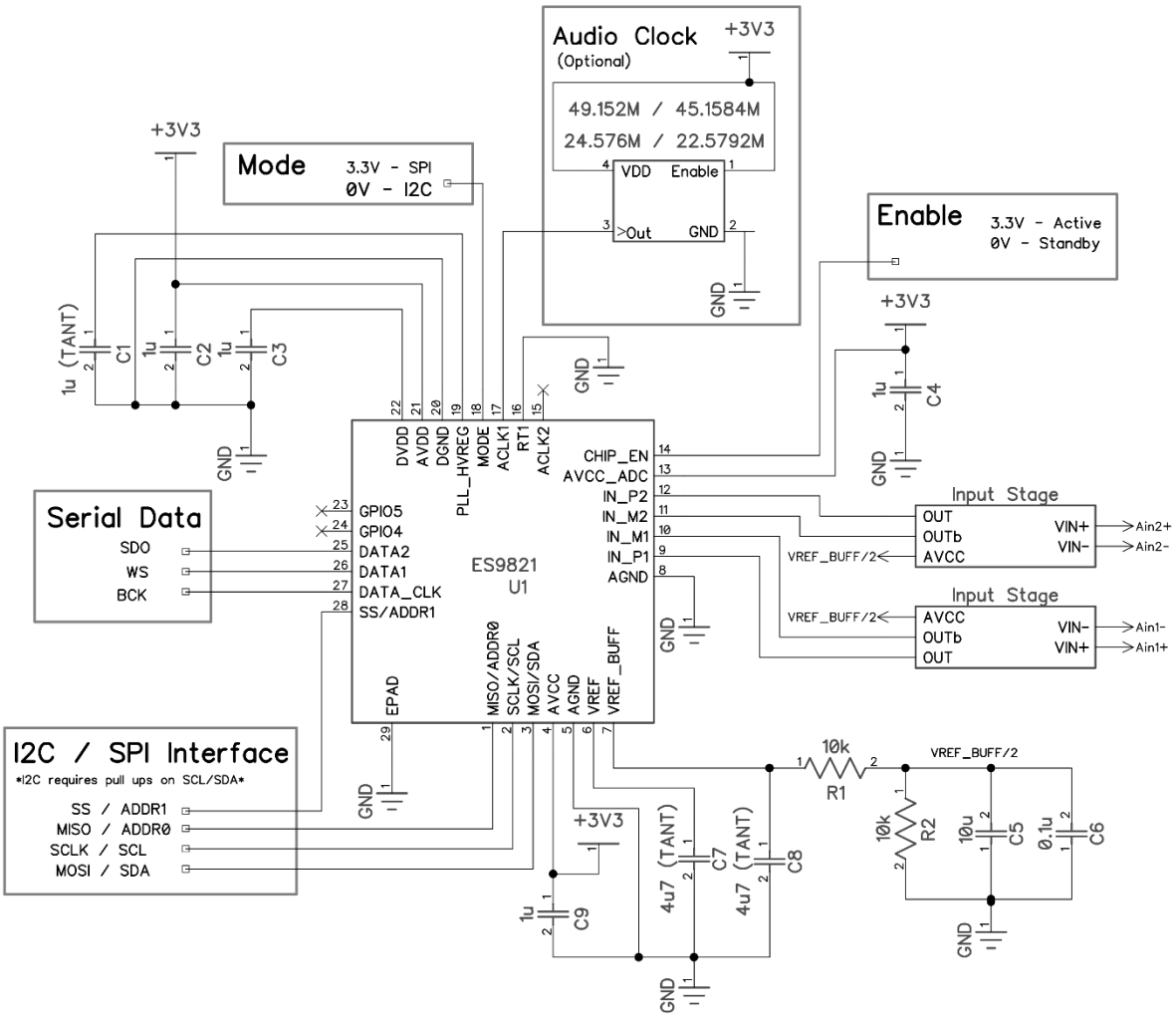


Figure 27 - ES9821Q Reference Schematic for Normal Operation in Software (SW) Mode
Schematic subject to change

Note: Pullup resistors are required on the SCL/SDA pins if using the I²C interface

Note: It is recommended to use Tantalum capacitors (where indicated) to achieve the highest performance

[6] Pin 29 QFN Package Pad (EPAD) should be connected to DGND.

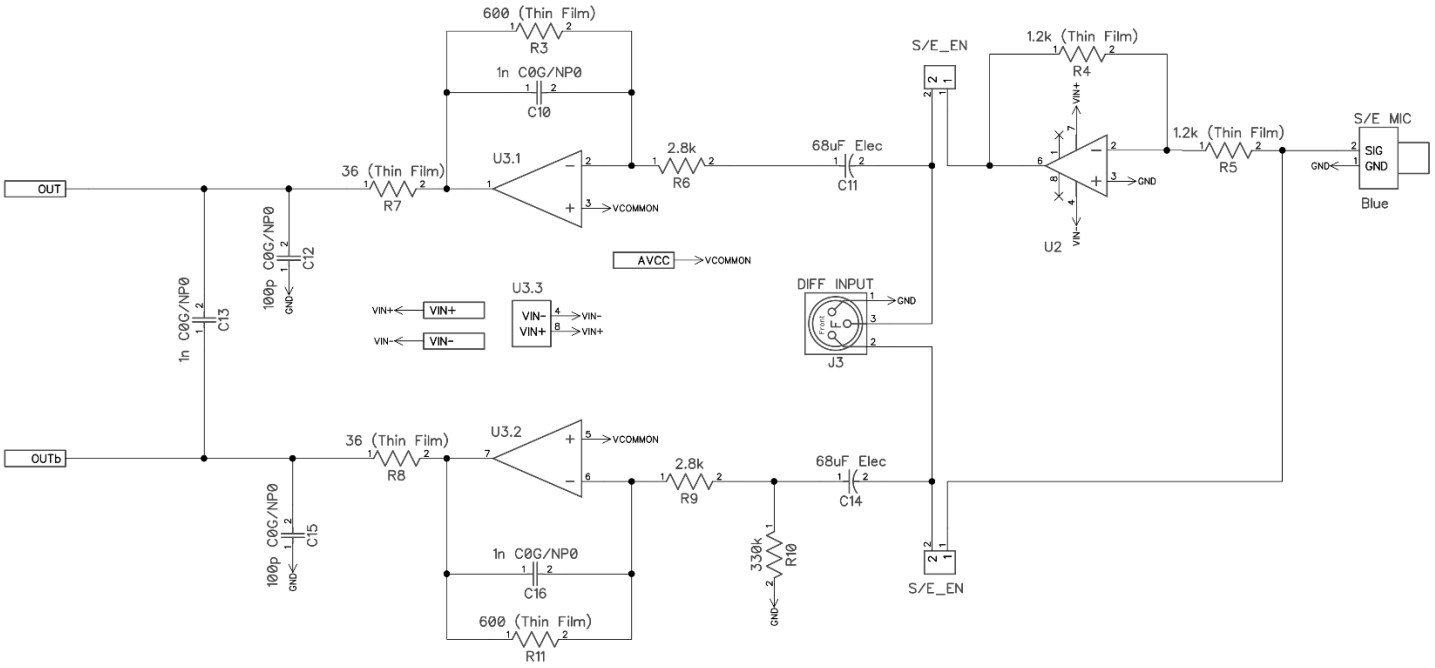


Figure 28 - Reference Schematic ADC Input Stage for Single Ended (S/E) and Differential Input

ES9821 PCB Layout Guidelines

To maximize performance of the ES9821 ESS Technology makes the following PCB Layout recommendations:

1. Use of a 4+ layer PCB with an uninterrupted ground plane immediately beneath the chip. Both analog and digital ground signal can be connected here.
2. All bypass capacitors to be placed as close to the chip as possible while keeping clear ground paths between them and the chip's ground pins.
3. The use of multiple vias for each supply near its bypass capacitor and chip ground pin.
4. Minimize the use of vias for high-speed data and clock lines and avoid routing them near or directly underneath the analog output signals.
5. Ensure the package pad is connected to ground plane on the back side of the PCB with multiple vias for heat dissipation.

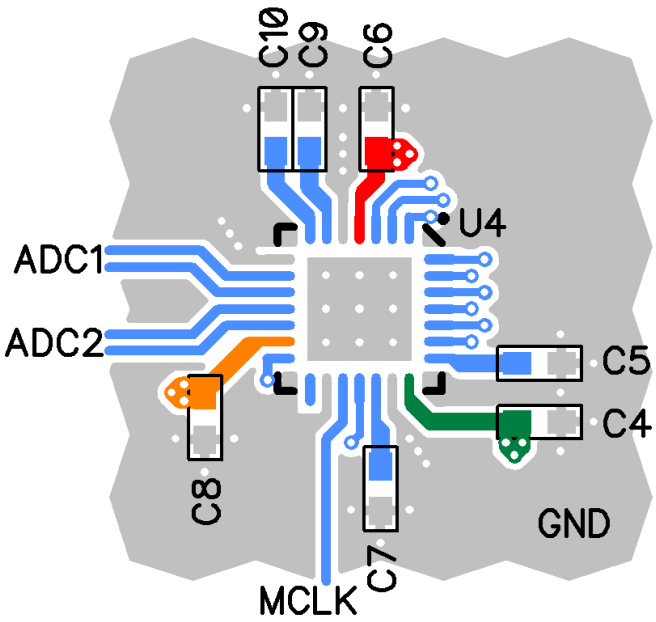
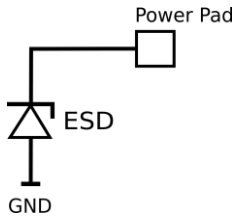
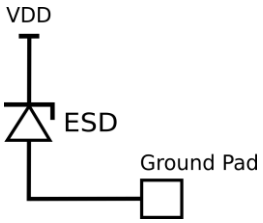
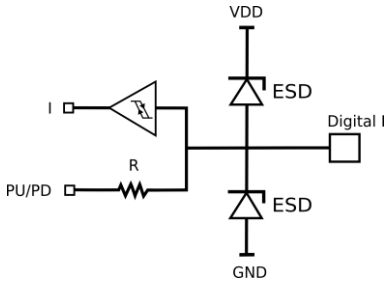
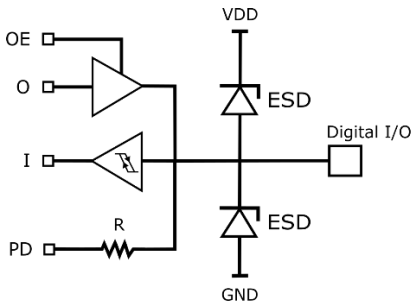


Figure 29 - ES9821 Recommended PCB Layout Guidelines

Internal Pad Circuitry

Pin Name	Type	Pin	Equivalent Circuit
AVCC_ADC AVDD AVCC	Power	13 21 4	
AGND AGND DGND	Ground	5 8 20	
CHIP_EN	Reset	14	
MISO/ADDR0/MUTE_MCLK_CTRL SCLK/SCL/HW1 MOSI/SDA/HW0 MODE GPIO5/HW4 GPIO4/HW3 DATA2/GPIO3 DATA1/GPIO2 DATA_CLK/GPIO1 SS/ADDR1/HW2	Digital I/O	1 2 3 18 23 24 25 26 27 28	

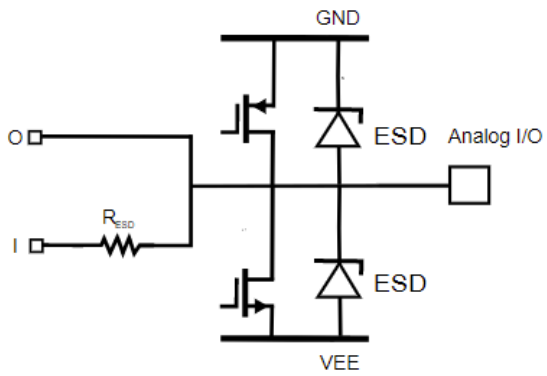
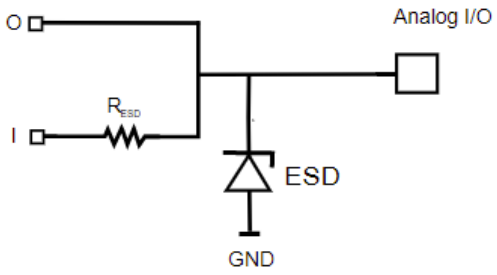
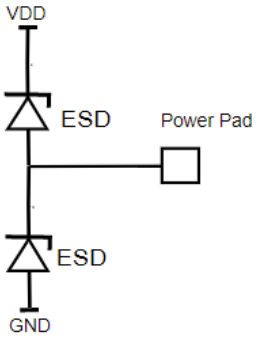
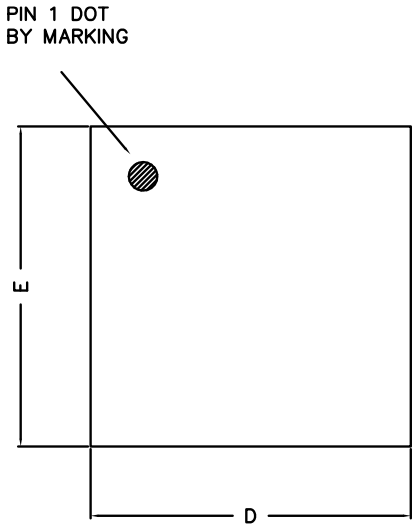
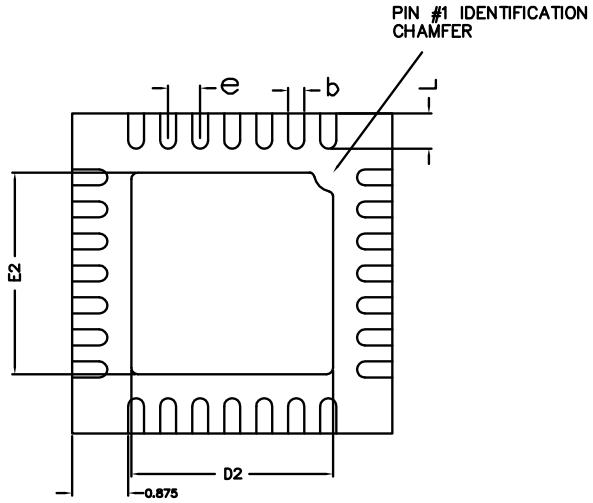
VREF VREF_BUF	Analog_IO_2 XVDD	6 7	
IN_P1 IN_P2 IN_M1 IN_M2	Analog IO ADC	9 12 10 11	
DVDD	IO Power	22	

Table 28 - Internal Pad Circuitry

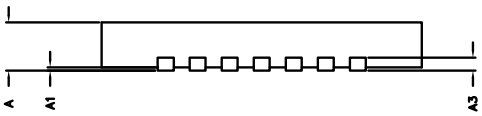
28 QFN Package Dimensions



TOP VIEW



BOTTOM VIEW

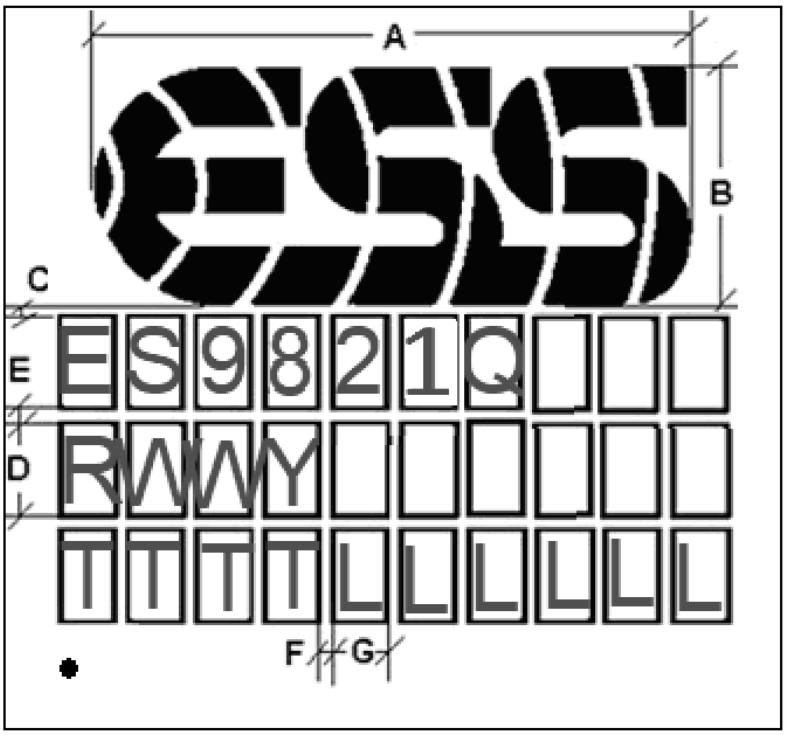


SIDE VIEW

COMMON DIMENSIONS			
PKG.	W: VERY VERY THIN		
REF.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3		0.2 REF.	
D	4.95	5.00	5.05
E	4.95	5.00	5.05
b	0.18	0.23	0.30
L	0.45	0.55	0.65
D2	3.00	3.15	3.25
E2	3.00	3.15	3.25
e		0.5 BSC	

Figure 30 - 28 QFN Package Dimensions

28 QFN Top View Marking



	Dimension in mm						
Package Type	A	B	C	D	E	F	G
QFN 5mm x 5mm	4.0	1.6	0.2	0.4	0.2	0.1	0.3

Mnemonic	Description
T	Tracking number
W	Work week
Y	Last digit of year
L	Lot number
R	Silicon Revision

Marking is subject to change. This drawing is not to scale.

Figure 31 - ES9821Q QFN Marking

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2 Pb-Free Process - Classification Temperatures (Tc)). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

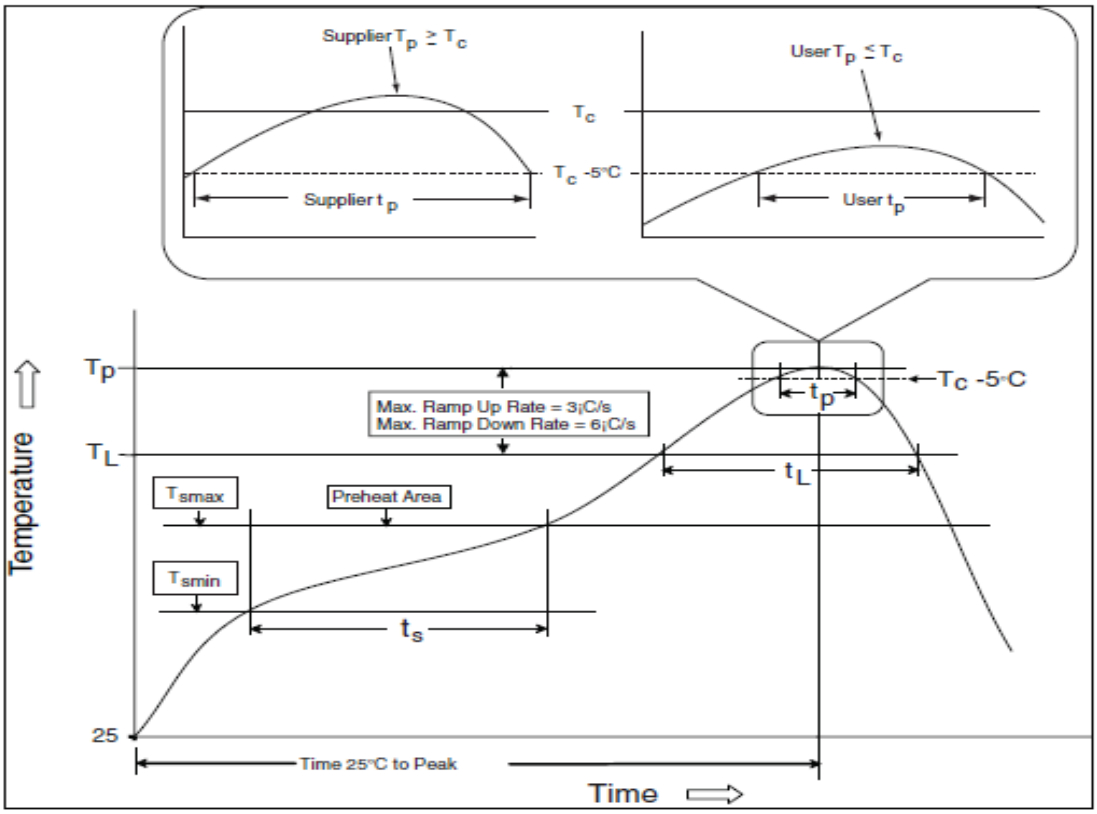


Figure 32 - IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350°C no longer than 3 seconds.

RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc), see Figure 28	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 29 - RPC-1 Classification Reflow Profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

RPC-2 Pb-Free Process - Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm - 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 30 - RPC-2 Pb Free Classification Temperatures

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9821Q	SABRE 32-bit 2 Channel ADC with built in digital filters, and multiple output formats	5mm x 5mm 28 QFN
ES9821QT* • **Inquire for availability**	ES9821Q with extended temperature range (-40 deg C to 105 deg C)	5mm x 5mm 28 QFN

Table 31 - Ordering Information

Revision History

Current Version 0.5.3

Rev.	Date	Notes
0.1.3	November 5, 2021	Initial release
0.2.1	September, 2022	• Reserved Register 12[6, 2], 194 • Unreserved Register 193[5:4]
0.3.1	February, 2023	• Unreserved Register 0[6:5], 193[0]
0.4.0	May, 2023	• Reserved HW modes 9-11, 13-15
0.5.0	December, 2024	• Unreserved Reg 63[1:0] and 64[1:0] • Added Power Up/Down Sequence
0.5.1	May, 2025	• Added Absolute maximum ratings for input pins • Added tolerances on Recommended Operating Conditions • Updated S/PDIF Audio Output Format • Unreserved Regs 18[4], 20[1]
0.5.2	June, 2025	• Updated the input impedance value
0.5.3	July, 2026	• Updated Pin Descriptions with required capacitor notes • Added PCB Layout Guidelines • Fixed APLL F_{VCO} equation and Updated Functional Block Diagram • Updated Recommended Power Up/Down Sequence with t_{data_out} • Replaced PDB with EN for Registers 195[0, 1], 200-202[23:22] • Added Bit-Clock (BCK) and Word-Select (WS) Timing • Updated Digital Filters • Renamed Clip Detector to Peak Detector. ○ Registers 12[5, 4, 1, 0], 26-28, 44, 45, 224[7, 6] • Updated Registers 237-240 with Peak equations