Analog Reinvented

ES9292PRO

Stereo Ultra-High Performance SMART CODEC

Product Datasheet

The SABRE® ES9292PRO is an Ultra-High performance stereo analog-to-digital (ADC) and digital-to-analog (DAC) SMART CODEC targeted for professional audio interfaces, very high-quality microphones, live stream media, powered speakers, mixers, recorders and other applications.

The ES9292PRO is a world class CODEC solution that has 2 integrated ADCs & DACs using ESS Technology's patented Hyperstream® IV Architecture, which delivers unprecedented audio quality and specifications, featuring a True Dynamic Range (DNR) of +128dB /+130dB and a THD+N of -118dB/-118dB for ADC/DAC, respectively, per channel. An analog-to-analog direct monitoring path with a mix mode is also provided with very low latency. The ES9292PRO supports I²S/LJ master/slave, TDM I/O, Native DSD, DoP, PDM & S/PDIF input/output. Custom pre-programmed filters including DC blocking that are complementary to both ADC & DAC are available along with Programmable FIR filters.

The SMART CODEC integrates a clock UPSAMPLER and patented Analog PLL that work together to recover audio clocks, minimize jitter and preserve signal integrity throughout the conversion chain while maintaining ADC & DAC performance. Along with ESS' 2nd generation Audio Signal Processors (ASP2) are incorporated on both ADC & DAC data paths, these features allow customers to target their audio requirements, by reducing BOM costs and optionally integrate multi-band PEQs, MIXERs, DRC, AGL, stereo widening, SABREXBASS enhancement and other specialty cross-over filters optimized with AI tools. ESS' SABRE Intelligence Studio (SI Studio) GUI with AI capability help simplify programming of the ASP2 and reduce or eliminate DSP requirements.

FEATURE	DESCRIPTION
+128dB/+130dB DNR per Channel (ADC/DAC) -118dB/-118dB THD+N per Channel (ADC/DAC)	Ultra-High performance with True Dynamic range and very low distortion for both input and output
High Sample Rates	Up to 768kHz PCM, DoP256 & DSD1024 in 64FS mode
2nd Generation Audio Signal Processor (ASP2)	For full customization of audio signaling requirements optimized with AI tools and SI Studio
UPSAMPLER and Patented Analog PLL	Low-jitter clocks while maintaining ADC & DAC performance
Direct Monitoring	Analog to Analog low latency direct monitoring
Multiple I/O Formats Available	I²S, TDM, DSD, DoP & PDM inputs/outputs are available, TDM daisy chain is supported as well as S/PDIF stereo input/output
Digital Volume Control (I²C/SPI) Digital Gain Control (I²C/SPI)	-127 to 0dB in increments of +0.5dB for ADC 0 to +42dB in increments of +6dB for creating maximum gain
I²C, SPI, and Hardware interface control	Configured by microcontroller or other I²C/SPI source, or pins through Hardware Mode for simplification of control
SPI Master	For control of external devices
Ultra-Low Noise Floor Bandwidth on ADC	200kHz bandwidth enabling higher resolution at higher sample rates
Integrated low noise reference regulators	Reduced BOM cost, PCB area and improved DNR
Customizable Filter Characteristics	Presets of digital optimal filters for ADC & DAC, programmability for custom filters is available
Low Pin Count Packaging	7mm x 7mm 48 pin QFN

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Functional Block Diagram

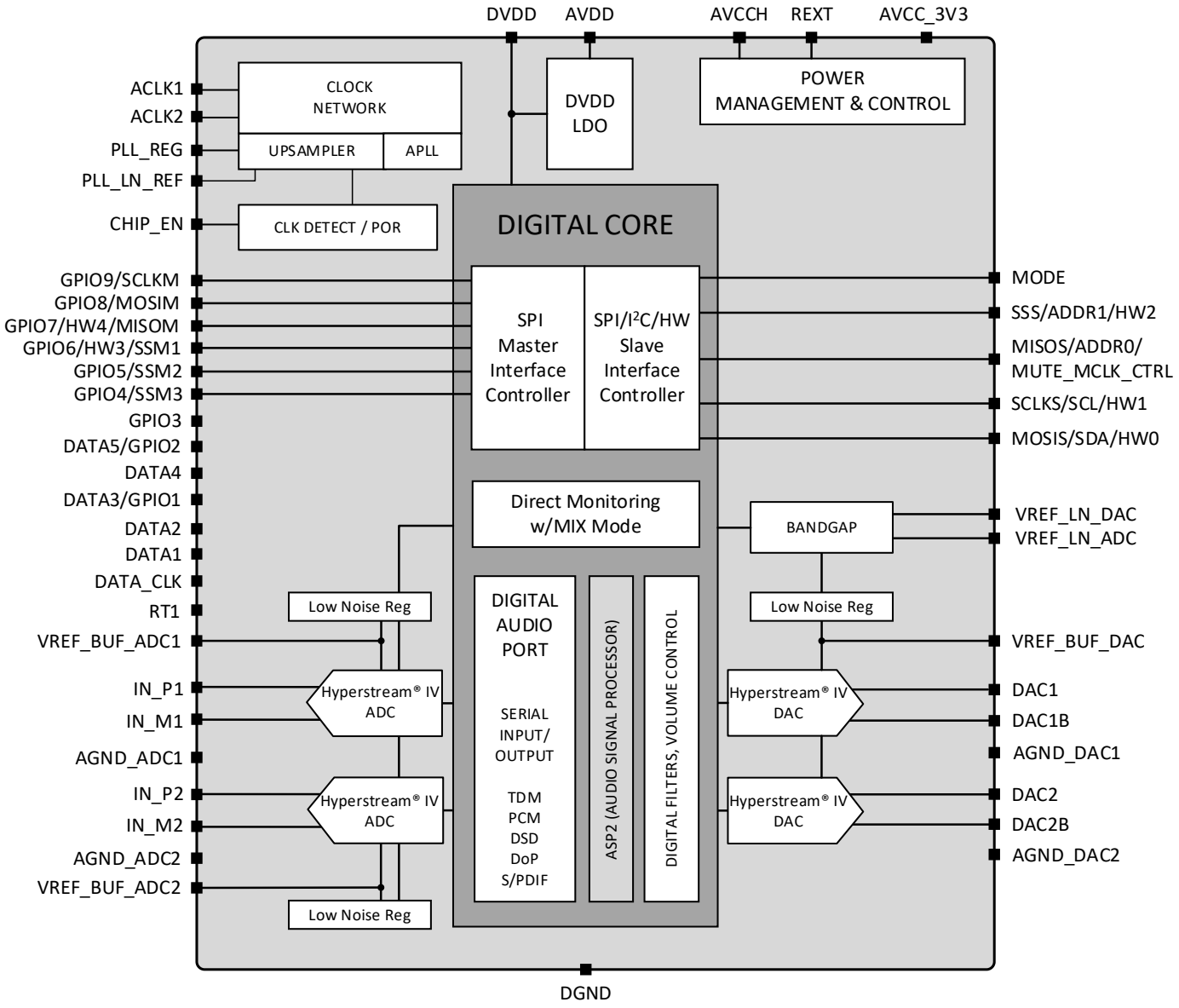


Figure 1 - ES9292PRO Functional Block Diagram

ES9292PRO Package

48QFN Pinout

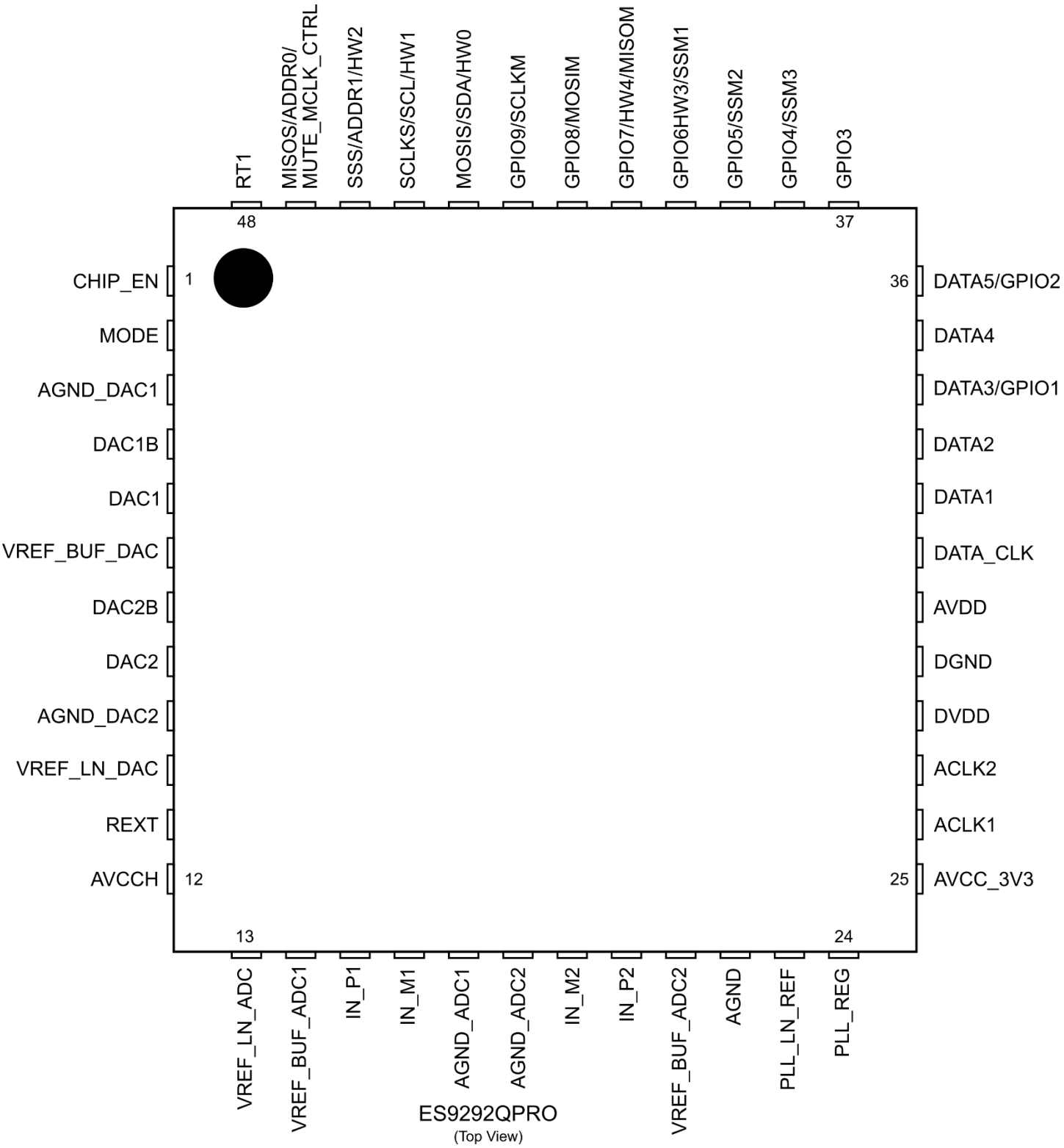


Figure 2 – ES9292QPRO 48QFN Pinout

48QFN Pin Descriptions

Pin	Name	Pin Type	Reset State	Pin Description
1	CHIP_EN	Reset	HiZ	Active-High Chip Enable
2	MODE	D I/O	HiZ	I²C/SPI Control selection or HW mode
3	AGND_DAC1	Ground	Ground	Analog Ground for DAC1
4	DAC1B	A O	Ground	DAC Channel 1 Differential Negative (-) Output
5	DAC1	A O	Ground	DAC Channel 1 Differential Positive (+) Output
6	VREF_BUF_DAC	A I/O	P/D	DAC Low Noise Supply. Internally Generated Requires external 1µF Tantalum and 100nF COG/NPO decoupling capacitors to ground. See Reference Schematic for details
7	DAC2B	A O	Ground	DAC Channel 2 Differential Negative (-) Output
8	DAC2	A O	Ground	DAC Channel 2 Differential Positive (+) Output
9	AGND_DAC2	Ground	Ground	Analog Ground for DAC2
10	VREF_LN_DAC	A I/O	P/D	DAC Low Noise Reference Voltage. Internally Generated. Requires an external 1µF Tantalum decoupling capacitor to ground. See Reference Schematic for details
11	REXT	A I/O	HiZ	External Power Supply Configuration Resistor.
12	AVCCH	Power	Power	Analog Supply. Requires an external 1µF Tantalum decoupling capacitor to ground. See Reference Schematic for details
13	VREF_LN_ADC	A I/O	P/D	ADC Low Noise Reference Voltage. Internally Generated. Requires an external 1µF Tantalum decoupling capacitor to ground. See Reference Schematic for details
14	VREF_BUF_ADC1	A I/O	P/D	ADC Channel 1 Low Noise Supply. Internally Generated. Requires external 1µF Tantalum and 100nF COG/NPO decoupling capacitors to ground. See Reference Schematic for details
15	IN_P1	A I	Ground	ADC Channel 1 Differential Positive (+) Input
16	IN_M1	A I	Ground	ADC Channel 1 Differential Negative (-) Input
17	AGND_ADC1	Ground	Ground	Analog Ground for ADC1
18	AGND_ADC2	Ground	Ground	Analog Ground for ADC2
19	IN_M2	A I	Ground	ADC Channel 2 Differential Negative (-) Input
20	IN_P2	A I	Ground	ADC Channel 2 Differential Positive (+) Input
21	VREF_BUF_ADC2	A I/O	P/D	ADC Channel 2 Low Noise Supply. Internally Generated.

				Requires external 1µF Tantalum and 100nF COG/NPO decoupling capacitors to ground. See Reference Schematic for details
22	AGND	Ground	Ground	Analog Ground
23	PLL_LN_REF	A O	P/D	PLL Low Noise Reference Voltage. Internally Generated. Requires an external 1µF Tantalum decoupling capacitor to ground. See Reference Schematic for details
24	PLL_REG	A O	P/D	Low Noise Supply for PLL. Internally generated. Requires external 1µF Tantalum and 100nF COG/NPO decoupling capacitors to ground. See Reference Schematic for details
25	AVCC_3V3	Power	Power	Analog 3.3V Supply
26	ACLK1	Clock I	HiZ	Clock Input 1
27	ACLK2	Clock I	Hiz	Clock Input 2
28	DVDD	A O	P/D	Digital core supply, internally generated Requires an external 1µF decoupling capacitor to ground. See Reference Schematic for details
29	DGND	Ground	Ground	Digital Ground
30	AVDD	Power	Power	I/O 3.3V Supply
31	DATA_CLK	D I/O	HiZ	Serial Data Clock
32	DATA1	D I/O	HiZ	Serial Data 1
33	DATA2	D I/O	HiZ	Serial Data 2
34	DATA3	D I/O	HiZ	Serial Data 3
	GPIO1			General I/O 1
35	DATA4	D I/O	HiZ	Serial Data 4
36	DATA5	D I/O	HiZ	Serial Data 5
	GPIO2			General I/O 2
37	GPIO3	D I/O	HiZ	General I/O 3
38	GPIO4	D I/O	HiZ	General I/O 4
	SSM3			SPI Slave Select (Master) pin #3, controlled by MODE Used for zero cross detection triggered SPI Master data.
39	GPIO5	D I/O	HiZ	General I/O 5
	SSM2			SPI Slave Select (Master) pin #2, controlled by MODE Used for zero cross detection triggered SPI Master data.
40	GPIO6	D I/O	HiZ	General I/O 6

	HW3			Hardware 3 interface pin, controlled by MODE
	SSM1			SPI Slave Select (Master) pin #1, controlled by MODE
41	GPIO7	D I/O	HiZ	General I/O 7
	HW4			Hardware 4 interface pin, controlled by MODE
	MISOM			SPI Main In Sub Out pin (Master), controlled by MODE
42	GPIO8	D I/O	HiZ	General I/O 8
	MOSIM			SPI Main Out Sub In pin (Master), controlled by MODE
43	GPIO9	D I/O	HiZ	General I/O 9
	SCLKM			SPI Serial Clock pin (Master), controlled by MODE
44	MOSIS	D I/O	HiZ	SPI Main Out Sub In pin (Slave), controlled by MODE
	SDA			I²C Serial Data pin, controlled by MODE
	HW0			Hardware 0 interface pin, controlled by MODE
45	SCLKS	D I/O	HiZ	SPI Serial Clock pin (Slave), controlled by MODE
	SCL			I²C Serial Clock pin, controlled by MODE
	HW1			Hardware 1 interface pin, controlled by MODE
46	SSS	D I/O	HiZ	SPI Slave Select pin (Slave), controlled by MODE
	ADDR1			I²C Address 1 pin, controlled by MODE
	HW2			Hardware 2 interface pin, controlled by MODE
47	MISOS	D I/O	HiZ	SPI Main In Sub Out pin (Slave), controlled by MODE
	ADDR0			I²C Address 0 pin, controlled by MODE
	MUTE_MCLK_CTRL			Hardware Mute Control pin, controlled by MODE
48	RT1	D I	HiZ	Reserved. **Must be connected to DGND for normal operation**.
49	Package Pad[1]	-	-	Electrically connected to internal grounds. **Must** be connected to ground.

Table 1 - 48QFN Pin List

[1] Pin 49 is the package pad. See 48 QFN package dimensions for sizing. Connect to DGND.

Feature List

- **+128dB True DNR for the ADC and +130dB True DNR for the DAC**
- **Clock Upsampler & APLL** - low-jitter clocks while maintaining ADC/DAC performance
- **ASP2 (2nd Generation Audio Signal Processor)** for both ADC and DAC custom signaling
- **Flexible I/O Support** — I²S, TDM, DSD, DoP, S/PDIF, PDM
- **High Sample rates**, up to 768kHz PCM, DoP256, DSD1024 supported
- **Independent Digital volume control** including up to +42dB of digital gain
- **Differential ADC input/DAC output** for improved noise immunity and common-mode rejection
- **SPI Master for control of external devices**

Configuration Modes

The ES9292PRO has 4 control programming modes which are controlled by the state of the MODE pin (Pin 2).

MODE PIN	Configuration
0	I²C Interface
Pull 0	HW control mode (see Hardware Mode Table)
Pull 1	HW control mode (see Hardware Mode Table)
1	SPI Interface

Table 2 - Mode Pin Configuration Options

Design Information

Hardware pins can be configured in 4 different ways. Each pin can be tied-high (1), pulled-high (Pull 1), pulled-low (Pull 0), or tied-low (0). HW0 and HW1 pins are always tied-high or tied-low. These 4 options also apply to MUTE_CTRL.

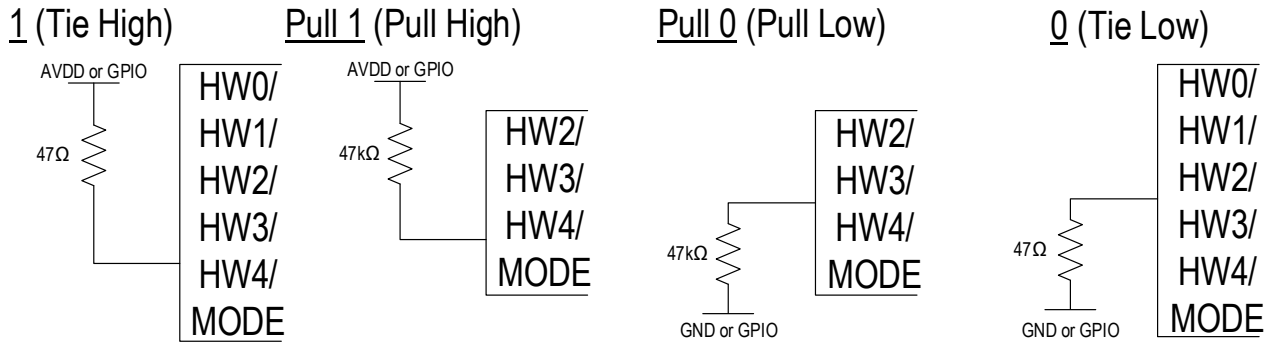


Figure 3 - Example Hardware Mode Pin Configurations

Software Mode

The ES9292PRO supports a slave I²C or SPI serial communication in software mode. There are two types of registers, read/write registers and read-only registers. Software modes are set when the MODE pin is a 0 (0V) for I²C or a 1 (AVDD) for SPI.

A system clock is not required to read and write registers.

I²C Slave Interface Commands

- MODE (Pin 2) – 0 (Tied-Low)
- Connect per I²C standard
  - SDA (Pin 44)
  - SCL (Pin 45)
  - ADDR0 (Pin 47)
  - ADDR1 (Pin 46)

I²C Address	ADDR1	ADDR0
0x30	GND	GND
0x32	GND	AVDD
0x34	AVDD	GND
0x36	AVDD	AVDD

Table 3 - I²C Addresses

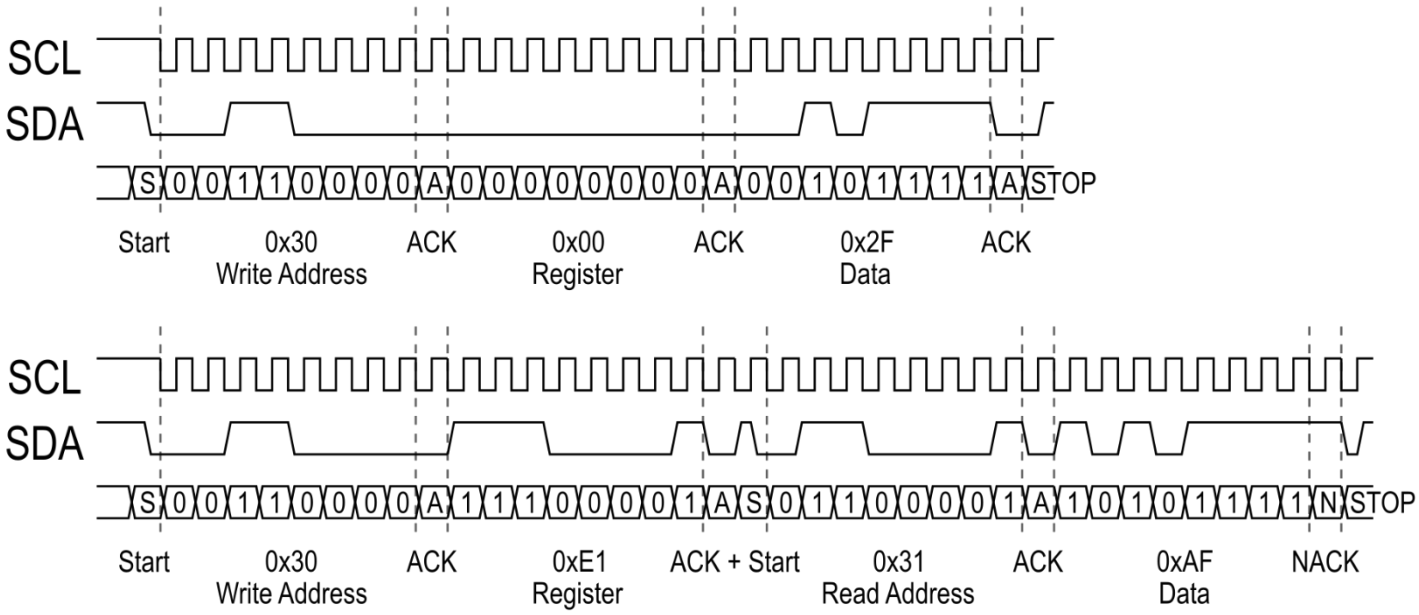


Figure 4 - I²C Write and Read Example

Note: CHIP_ID for the ES9292PRO is 0xAF in Register 225 (0xE1)

SPI Slave Interface Commands

- MODE (Pin 2) – 1 (Tied-High)
- Connect per SPI standard
  - MOSIS (Pin 44)
  - SCLKS (Pin 45)
  - SSS (Pin 46)
  - MISOS (Pin 47)

SPI Command	First Byte
Write	0x03
Read	0x01

Table 4 - SPI Commands

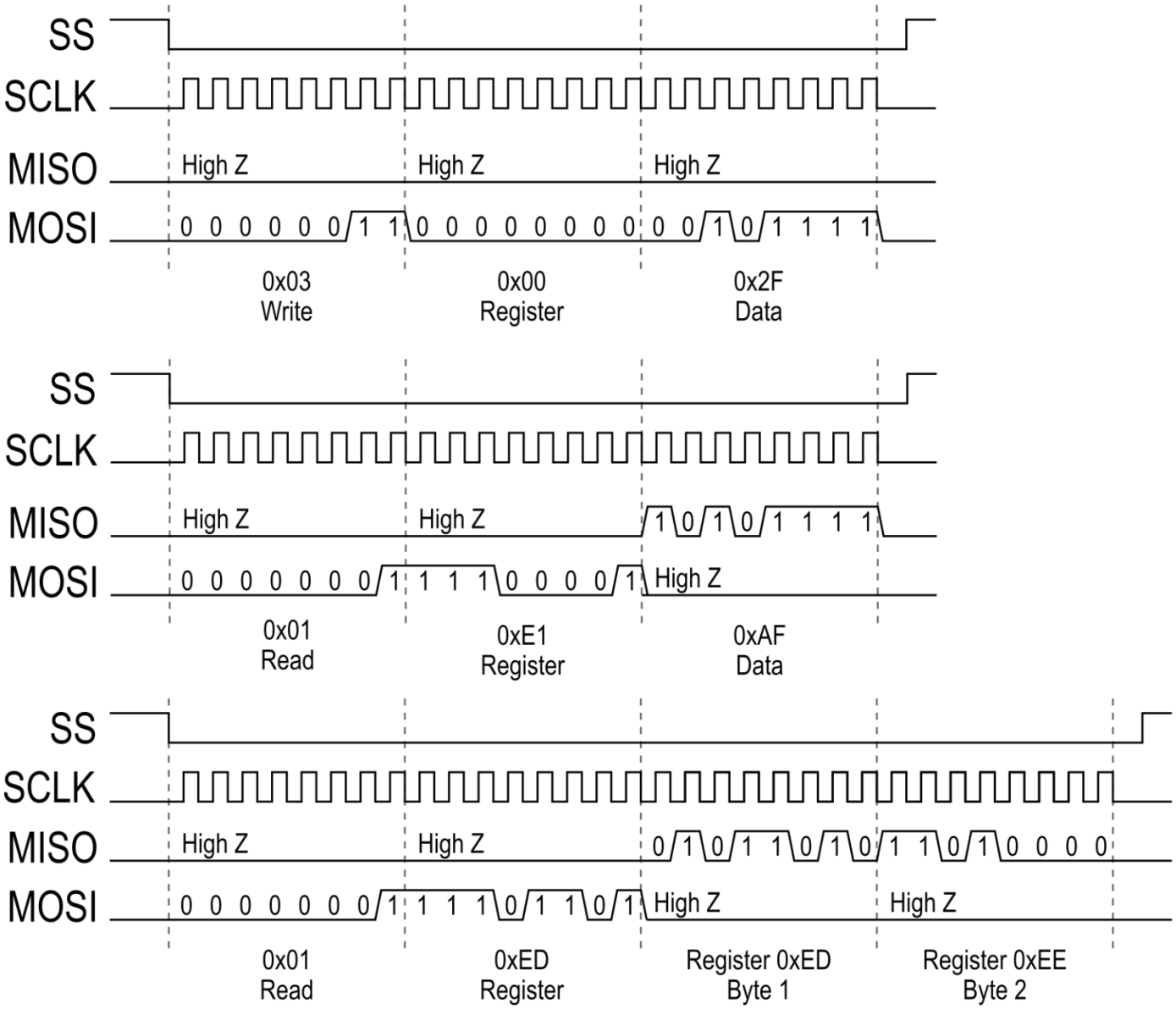


Figure 5 - SPI Write, Read, and Multi-byte Read Example

Note: CHIP_ID for the ES9292PRO is 0xAF in Register 225 (0xE1)

MCLK Control

In Software Modes, Register 6[4] MCLK_24M_DIV2 must be set correctly according to the external MCLK being used.

MCLK_24M_DIV2	MCLK
0	24.576MHz/22.5792MHz
1	49.152MHz/45.1584MHz

Table 5 - MCLK Control in Software Mode

Hardware Mode

The ES9292PRO has pre-configured modes that can be set with an external pin configuration. These modes configure the DAC for different input/output serial data rates and set the mute control. Hardware modes also support stereo digital PDM microphones as inputs. Each hardware mode pin has 4 states that can be found in Design Information.

These modes are set with pins:

- MODE (Pin 2)
- HW0 (Pin 44)
- HW1 (Pin 45)
- HW2 (Pin 46)
- HW3 (Pin 40)
- HW4 (Pin 41)
- MUTE_MCLK_CTRL (Pin 47)

Recommended Hardware Mode Setup Sequence

The Hardware Mode setup sequence is shown below with all hardware pins being defined after CHIP_EN is asserted.

Note: MUTE_CTRL should be set to muted until the HW mode is finalized and after CHIP_EN is asserted, then it may be set to the correct clock rate and unmuted last. See Mute and MCLK Control for more information.

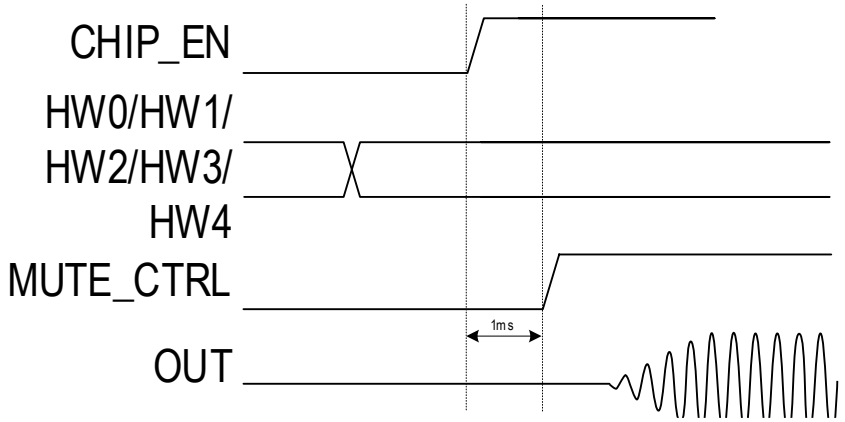


Figure 6 - Hardware Mode Startup Sequence

Hardware Pin Configurations

HW #	Mode Description	FS [kHz]	BCK [MHz]	BCK/Channel	Channel Slots	MCLK [MHz]	Mode	HW2	HW1	HW0
32-bit PCM & DoP[1] Master Modes										
0	I2S with Ext MCLK DoP64/128	MCLK/128	MCLK/2 (64*FS)	32	1, 2	128*FS	Pull 0	0	0	0
1	I2S with Ext MCLK DoP64	MCLK/256	MCLK/4 (64*FS)	32	1, 2	256*FS	Pull 0	0	0	1
2	I2S with Ext MCLK	MCLK/512	MCLK/8 (64*FS)	32	1, 2	512*FS	Pull 0	0	1	0
3	I2S with Ext MCLK	MCLK/1024	MCLK/16 (64*FS)	32	1, 2	1024*FS	Pull 0	0	1	1
4	LJ with Ext MCLK DoP64/128	MCLK/128	MCLK/2 (64*FS)	32	1, 2	128*FS	Pull 0	Pull 0	0	0
5	LJ with Ext MCLK DoP64	MCLK/256	MCLK/4 (64*FS)	32	1, 2	256*FS	Pull 0	Pull 0	0	1
6	LJ with Ext MCLK	MCLK/512	MCLK/8 (64*FS)	32	1, 2	512*FS	Pull 0	Pull 0	1	0
7	LJ with Ext MCLK	MCLK/1024	MCLK/16 (64*FS)	32	1, 2	1024*FS	Pull 0	Pull 0	1	1
32-bit PCM & DoP[1] Slave Modes, Auto FS Detect & PLL										
8	I2S Slave, Auto FS DoP64/128	22.05 ≤ FS ≤ 768	64*FS	32	1, 2	22.5792 / 24.576 45.1584 / 49.152	Pull 0	Pull 1	0	0
9	I2S Slave, PLL MCLK	44.1 / 48	3.072	32	1, 2	22.5792 / 24.576 45.1584 / 49.152 From PLL	Pull 0	Pull 1	0	1
10	I2S Slave, PLL MCLK	88.2 / 96	6.144	32	1, 2		Pull 0	Pull 1	1	0
11	I2S Slave, PLL MCLK DoP64	176.4 / 192	12.288	32	1, 2		Pull 0	Pull 1	1	1
12	LJ Slave, Auto FS DoP64/128	22.05 ≤ FS ≤ 768	64*FS	32	1, 2	22.5792 / 24.576 45.1584 / 49.152	Pull 0	1	0	0
13	LJ Slave, PLL MCLK	44.1 / 48	3.072	32	1, 2	22.5792 / 24.576 45.1584 / 49.152 From PLL	Pull 0	1	0	1
14	LJ Slave, PLL MCLK	88.2 / 96	6.144	32	1, 2		Pull 0	1	1	0
15	LJ Slave, PLL MCLK DoP64	176.4 / 192	12.288	32	1, 2		Pull 0	1	1	1

Table 6 - Hardware Mode Pin Configurations

[1] The DAC will automatically switch between DoP and PCM/TDM depending on the format detected from the signal. The ADC must be set to DoP using the HW3 pin.

Hardware Mode Pin Configurations Continued

HW #	Mode Description	FS [kHz]	BCK [MHz]	BCK/Channel	Channel Slots	MCLK [MHz]	Mode	HW2	HW1	HW0
32-bit TDM LJ Slave Modes, Auto FS & CH Num										
16	32-bit TDM LJ Slave Auto FS Auto CH Num	22.05 ≤ FS ≤ 768	Auto(128FS, 256FS, 512FS, 1024FS)	32	1, 2	22.5792 / 24.576 45.1584 / 49.152	Pull 1	0	0	0
17		22.05 ≤ FS ≤ 384	Auto(256FS, 512FS, 1024FS)	32	3, 4		Pull 1	0	0	1
18		22.05 ≤ FS ≤ 192	Auto(512FS, 1024FS)	32	5, 6		Pull 1	0	1	0
19		22.05 ≤ FS ≤ 192	Auto(512FS, 1024FS)	32	7, 8		Pull 1	0	1	1
20		22.05 ≤ FS ≤ 96	Auto(1024FS)	32	9, 10		Pull 1	Pull 0	0	0
21		22.05 ≤ FS ≤ 96	Auto(1024FS)	32	11, 12		Pull 1	Pull 0	0	1
22		22.05 ≤ FS ≤ 96	Auto(1024FS)	32	13, 14		Pull 1	Pull 0	1	0
23		22.05 ≤ FS ≤ 96	Auto(1024FS)	32	15, 16		Pull 1	Pull 0	1	1
DSD Master, DSD Slave, I2S/LJ Slave Mono, S/PDIF w/ PLL										
24	DSD / PDM Master	DSD512, PDM512	512*FS	-	-	22.5792 / 24.576 45.1584 / 49.152	Pull 1	Pull 1	0	0
25		DSD256, PDM256	256*FS	-	-		Pull 1	Pull 1	0	1
26		DSD128, PDM128	128*FS	-	-		Pull 1	Pull 1	1	0
27		DSD64, PDM64	64*FS	-	-		Pull 1	Pull 1	1	1
28	DSD / PDM Slave	DCLK / 64	DSD64-DSD512	-	-		Pull 1	1	0	0
29	I2S Slave, Mono	22.05 ≤ FS ≤ 768	64*FS	32	1 or 2		Pull 1	1	0	1
30	LJ Slave, Mono	22.05 ≤ FS ≤ 768	64*FS	32	1 or 2		Pull 1	1	1	0
31	S/PDIF, PLL	16 ≤ FS ≤ 192	-	-	1, 2	22.5792 / 24.576 45.1584 / 49.152 from PLL **@ 50MHz on ACLK2**	Pull 1	1	1	1

Table 7 - Hardware Mode Pin Configuration Continued

GPIO Functions in Hardware Mode

Supported HW Modes	HW3 (Pin 27)	DAC Filter Select	Other Control
0 – 15	0	Filter 1 Minimum Phase	ADC DoP[1] Disabled
	Pull 0		ADC DoP[1] Enabled
	Pull 1	Filter 3 Linear Phase Fast Roll-Off	ADC DoP[1] Disabled
	1		ADC DoP[1] Enabled
16-23	0	Filter 1 Minimum Phase	Parallel
	Pull 0		Daisy Chain
	Pull 1	Filter 3 Linear Phase Fast Roll-Off	Parallel
	1		Daisy Chain
24-28	0 / Pull 1	-	PDM Disabled
	Pull 0 /1		PDM Enabled
29, 30	0	Filter 1 Minimum Phase	Mono Slot 1
	Pull 0		Mono Slot 2
	Pull 1	Filter 3 Linear Phase Fast Roll-Off	Mono Slot 1
	1		Mono Slot 2
31	0 / Pull 0	Filter 1 Minimum Phase	-
	Pull 1 / 1	Filter 3 Linear Phase Fast Roll-Off	

Table 8 - DAC Filter, DoP, Daisy Chain, PDM, Mono control with HW3

Supported HW Modes	HW4 (Pin 41)	DAC Automute	ADC DC Block
All	0	Disabled	Disabled
	Pull 0	Disabled	Enabled
	Pull 1	Enabled	Disabled
	1	Enabled	Enabled

Table 9 - DAC Automute and ADC DC Block control with HW4

GPIO5 (Pin 39)	ADC Input	GPIO4 (Pin 36)	GPIO3 (Pin 35)	ADC Gain
0	Analog	0	0	+0dB
		0	1	+18dB
		1	0	+24dB
		1	1	+30dB
1	PDM Microphone	PDM_MIC_DATA [I]	PDM_MIC_CLK[O]	-

Table 10 - ADC Input Select and Gain control with GPIO5/4/3

[1] DoP is only supported in HW Modes 1, 2, 4, 5, 8, 11, 12, and 15.

Mute and MCLK Control

Set MUTE_MCLK_CTRL (Pin 47) to mute the output while in Hardware Mode:

MUTE_MCLK_CTRL (Pin 47)	Condition	MCLK
0	Mute	24.576MHz
1	Unmute	24.576MHz
Pull 0	Mute	49.152MHz
Pull 1	Unmute	49.152MHz

Table 11 - Mute and MCLK Control in Hardware Mode

Note: In Hardware Modes 9-11, 13-15, the state of MUTE_MCLK_CTRL will determine the output PLL rate.

Note: If MUTE_MCLK_CTRL (Pin 47) is set to the incorrect MCLK rate, the ADC may have less output performance.

Digital Features

Audio Input/Output Formats

The ES9292PRO supports multiple audio serial input and output data formats and are selected through either Software or Hardware modes.

The ES9292PRO DAC datapath supports PCM/TDM, DSD, PDM, DoP and S/PDIF input formats and is selected using Register 4[3:1] INPUT_DATA_FORMAT_SEL in software mode. The corresponding ENABLE_[data_format]_DECODE bit in Register 2 or 4 must also be set. The input data format can be automatically determined, apart from PDM, with the use of Register 4[0] AUTO_INPUT_FORMAT_SEL

The ES9292PRO ADC datapath supports PCM/TDM, DSD, PDM, DoP and S/PDIF output formats along with Analog/PDM microphone input formats selected using Register 3[3:1] OUTPUT_DATA_FORMAT_SEL and Register 3[6] ENABLE_PDM_MIC_DECODE respectfully. The corresponding ENABLE_[data_format]_ENCODE bit in Register 2 or 3 must also be set. The output data format can be configured to follow the set input data format using Register 3[0] OUPUT_FMT_FLW_INPUT. The formats include:

- PCM
  - Slave and master mode is 16, 24, 32 – bit widths (32-bit in HW Mode)
  - I²S and Left-Justified (LJ)
  - Sample rates up to 768kHz (64fs mode)
  - Channel mapping
- TDM
  - Up to 32 slots including daisy chain mode (16-slot in HW Mode)
  - Slave mode in hardware mode. Slave and master modes in software mode
  - LJ Format in hardware modes, I²S or LJ in software modes
  - Channel mapping
- DSD
  - Slave and master modes in software mode
  - Sample rates from DSD64 (2.8224Mbits/s, 64x44.1kHz) to DSD1024
  - Channel mapping
- DoP (DSD over PCM)
  - Slave and master modes in software mode
  - Sample rates from DoP64 to DoP256
  - Channel mapping
- PDM
  - Slave and master modes in software mode
  - Sample rates from PDM64 to PDM512
- S/PDIF
  - Stereo 2 Channel Output
  - Input Selection
  - Sample rates up to 192kHz
- PDM Microphone Input
  - Master mode in hardware and software mode
  - Sample rates from PDM64 to PDM512

PCM (I2S, LJ) Format

PCM includes I²S and LJ with 2 channels/slots per data line. The ADC outputs can be mapped to any slot/channel of the PCM encoder output data (DATA2) using TDM_ENC_SLOT_SEL_CHx. The PCM decoder routes any slot/channel of the PCM input data (DATA4) to the DACs using TDM_DEC_SLOT_SEL_CHx.

Pin Name	Function	Direction	Description
DATA_CLK	PCM BCLK	[I/O]	PCM Clock (Bit Clock), Master or Slave
DATA1	PCM WS	[I/O]	PCM WS (Word Select/Frame Select), Master or Slave
DATA2	PCM ENC DATA1	[O]	PCM Data Output from ADC (Encoder)
DATA4	PCM DEC DATA1	[I]	PCM Data Input for DAC (Decoder)

Table 12 - PCM Pin Connections

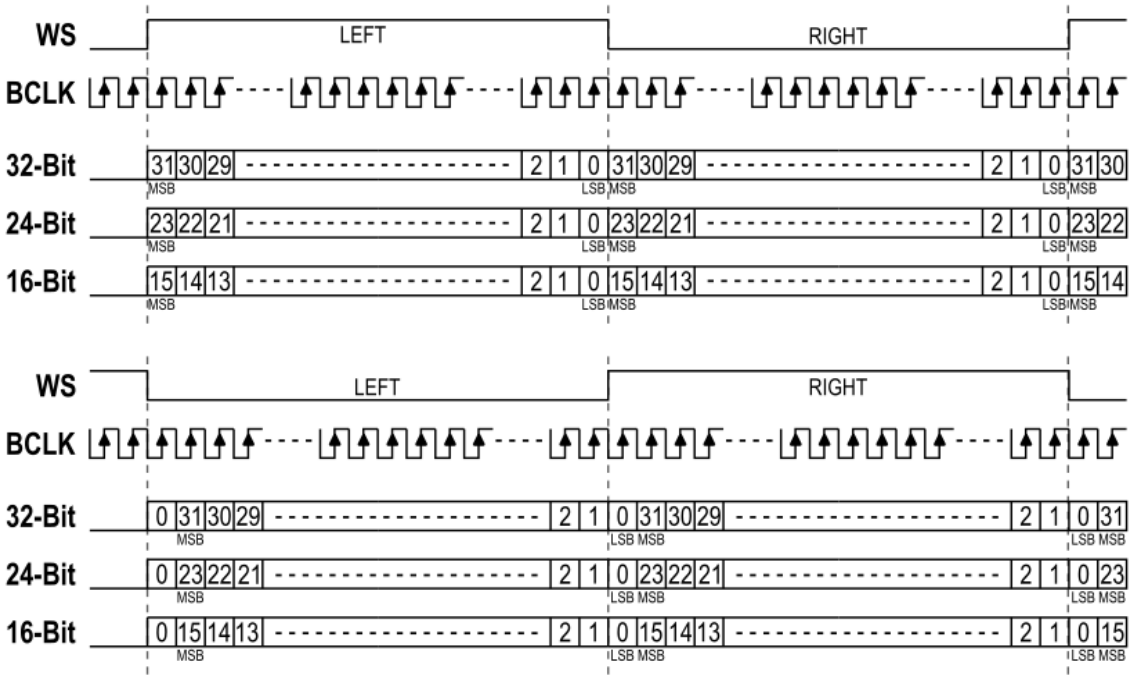


Table 13 - LJ (top) & I2S (bottom) for 32, 24, and 16-bit Word Widths

TDM Format

The ES9292PRO supports TDM format, allowing more than 2 channels/slots to be transmitted and received on a data line, up to a maximum of 32 channels. Supported formats are TDM4 (4ch), TDM8 (8ch), TDM16 (16ch) and TDM32 (32ch). The ADC outputs can be mapped to any slot of the TDM output data (DATA2) using TDM_ENC_SLOT_SEL_CHx. The DACs can choose any slot/channel of the TDM input data (DATA4) using TDM_DEC_SLOT_SEL_CHx.

Data is latched on the positive edge of BCLK.

Pin Name	Function	Direction	Description
DATA_CLK	TDM BCLK	[I/O]	TDM Clock, Master or Slave
DATA1	TDM WS	[I/O]	TDM WS, Master or Slave
DATA2	TDM ENC DATA1	[O]	TDM Encoder Channel 1 & 2 (default)
GPIO1/DATA3	TDM ENC DAISY	[I]	TDM Encoder Daisy Chain Pin
DATA4	TDM DEC DATA1	[I]	TDM Decoder Channel 1 & 2 (default)
GPIO2/DATA5	TDM DEC DAISY	[O]	TDM Decoder Daisy Chain Pin

Table 14 - TDM Pin Connections

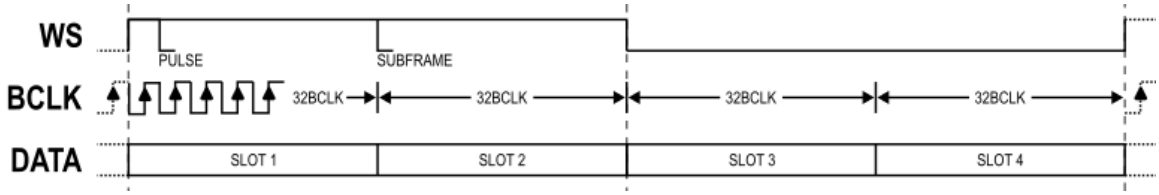


Figure 7 - TDM4 Mode

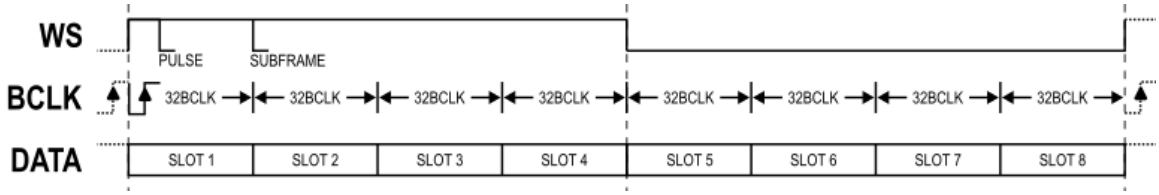


Figure 8 - TDM8 Mode

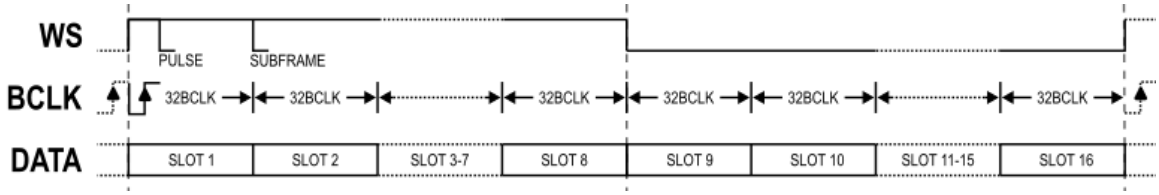


Figure 9 - TDM16 Mode

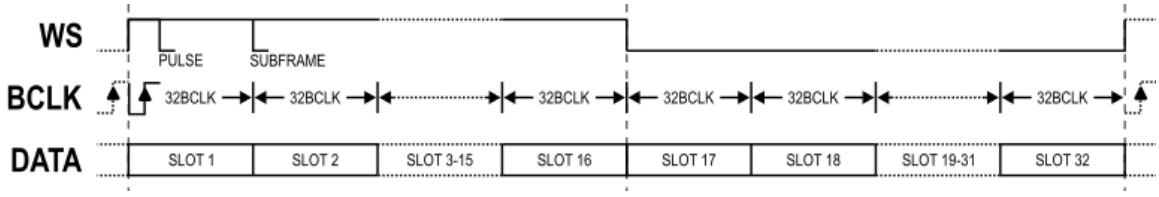


Figure 10 - TDM32 Mode

PCM/TDM Encoder

The ES9292PRO integrates a 2 channel 1 line PCM/TDM Encoder whose output has a maximum word width of 32-bits (default) and a maximum bit depth of 32-bit (default). The encoder allows for I²S, LJ, and TDM output streams.

The PCM/TDM Encoder can support up to 32 different slots and each channel for the ADC can be mapped to any of the 32 slots.

Note: The PCM/TDM Encoder and PCM/TDM Decoder share the same formatting registers settings.

Note: the PCM/TDM Encoder supports Right Justified (RJ) format in software mode for a single device using TDM_ENC_DATA_LATCH_ADJ.

PCM/TDM Encoder Formatting Registers

- Register 2[0] ENABLE_TDM_ENCODE = 1'b1
- Register 3[3:1] OUTPUT_DATA_FORMAT_SEL = 3'b000 (PCM/TDM)
- Register 10[6] AUTO_CH_DETECT
- Register 10[4:0] TDM_CH_NUM
- Register 11[6] NOISE_FLOOR_SHAPE_16BIT
- Register 11[5:4] TDM_WORD_WIDTH
- Register 11[3:2] TDM_BIT_DEPTH
- Register 11[1] TDM_VALID_EDGE
- Register 11[0] TDM_LJ

PCM/TDM Encoder Mapping Registers

- Register 12-13[4:0] TDM_ENC_SLOT_SEL_CH1
- Register 12-13[12:8] TDM_ENC_SLOT_SEL_CH2

PCM/TDM Encoder Daisy Chain Registers

- Register 16[7] TDM_ENC_DAISY_CHAIN
- Register 16[4:0] TDM_ENC_DATA_LATCH_ADJ

PCM/TDM Decoder

The ES9292PRO integrates a 2 channel 1 line PCM/TDM Decoder whose input has a maximum word width of 32-bits (default) and a maximum bit depth of 32-bit (default). The decoder allows for I²S, LJ, and TDM output streams.

The PCM/TDM Decoder can support up to 32 different slots and each channel for the DAC can be mapped to any of the 32 slots.

Note: The PCM/TDM Encoder and PCM/TDM Decoder share the same formatting registers settings.

Note: the PCM/TDM Decoder supports Right Justified (RJ) format in software mode for a single device using TDM_DEC_DATA_LATCH_ADJ.

PCM/TDM Decoder Formatting Registers

- Register 2[4] ENABLE_TDM_DECODE = 1'b1
- Register 4[3:1] INPUT_DATA_FORMAT_SEL = 3'b000 (PCM/TDM)
    - Or Register 4[0] AUTO_INPUT_FORMAT_SEL = 1'b1
- Register 10[6] AUTO_CH_DETECT
- Register 10[4:0] TDM_CH_NUM
- Register 11[6] NOISE_FLOOR_SHAPE_16BIT
- Register 11[5:4] TDM_WORD_WIDTH
- Register 11[3:2] TDM_BIT_DEPTH
- Register 11[1] TDM_VALID_EDGE
- Register 11[0] TDM_LJ

PCM/TDM Decoder Mapping Registers

- Register 14-15[4:0] TDM_DEC_SLOT_SEL_CH1
- Register 14-15[12:8] TDM_DEC_SLOT_SEL_CH2

PCM/TDM Decoder Daisy Chain Registers

- Register 17[7] TDM_DEC_DAISY_CHAIN
- Register 17[4:0] TDM_DEC_DATA_LATCH_ADJ

DSD Format

The ES9292PRO features the DSD format with rates from DSD64 to DSD512.

Pin Name	Function	Direction	Description
DATA_CLK	DSD CLK	[I/O]	DSD Clock
DATA2	DSD ENC CH1	[O]	DSD Encoder Channel 1 (default)
GPIO1/DATA3	DSD ENC CH2	[O]	DSD Encoder Channel 2 (default)
DATA4	DSD DEC CH1	[I]	DSD Decoder Channel 1 (default)
GPIO2/DATA5	DSD DEC CH2	[I]	DSD Decoder Channel 2 (default)

Table 15 - DSD Pin Connections

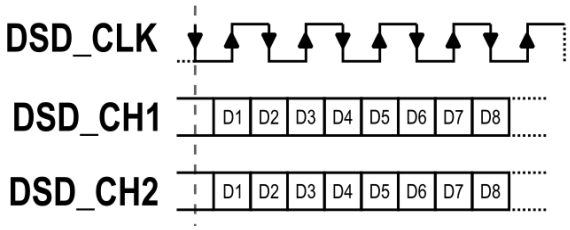


Figure 11 - DSD Format, 1-bit stream

DSD Encoder

The ES9292PRO integrates a DSD Encoder output from the ADC datapath with a single clock line and dual data lines. Each data line can be mapped to either ADC channel with the remapping registers.

DSD Encoder Registers

- Register 2[2] ENABLE_DSD_ENCODE = 1'b1
- Register 3[3:1] OUTPUT_DATA_FORMAT_SEL = 3'b010

DSD Encoder Mapping Registers

- Register 18[0] DSD_ENC_CH_SEL_DATA2
- Register 18[1] DSD_ENC_CH_SEL_DATA3

DSD Decoder

The ES9292PRO integrates a DSD Decoder input into the DAC datapath with a single clock line and dual data lines. Each DSD source can be remapped to any DAC channel by using the remapping registers.

DSD Decoder Registers

- Register 2[6] ENABLE_DSD_DECODE = 1'b1
- Register 3[3:1] INPUT_DATA_FORMAT_SEL = 3'b010
    - Or Register 4[0] AUTO_INPUT_FORMAT_SEL = 1'b1

DSD Decoder Mapping Registers

- Register 18[4] DSD_DEC_LINE_SEL_CH1
- Register 18[5] DSD_DEC_LINE_SEL_CH2

DoP Format

The ES9292PRO features the DoP format with rates from DoP64 to DoP256. DoP encoders 16 bits of DSD data into a 24-bit PCM frame, with the 8 most significant bits containing the DSD marker. The marker alternates between 0x05 and 0xFA every sample. The DSD data is inserted into the frame such that the oldest bit is in the t_0 position.

Pin Name	Function	Direction	Description
DATA_CLK	DoP BCLK	[I/O]	DoP Clock, Master or Slave
DATA1	DoP WS	[I/O]	DoP WS, Master or Slave
DATA2	DoP ENC DATA1	[O]	DoP Encoder Data Channel 1 & 2
DATA4	DoP DEC DATA1	[I]	DoP Decoder Data Channel 1 & 2

Table 16 - DoP Pin Connections

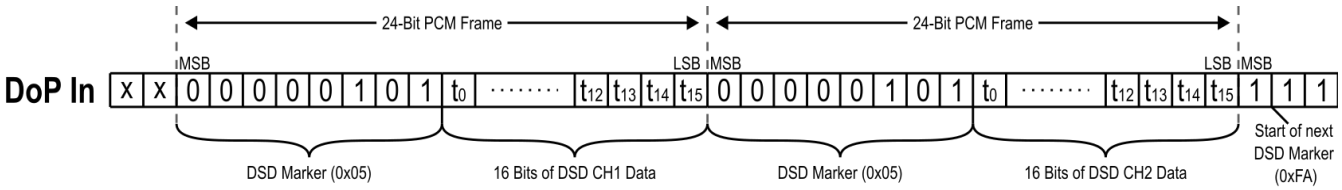


Figure 12 - DoP Format

DoP Encoder

The ES9292PRO integrates a DoP (DSD over PCM) Encoder that converts the DSD data from the DSD datapath into DoP internally. The channels can be remapped by using the PCM/TDM Encoder Mapping Registers.

DoP Decoder Registers

- Register 2[2] ENABLE_DOP_ENCODE = 1'b1
- Register 2[0] ENABLE_TDM_ENCODE = 1'b1
- Register 3[3:1] OUTPUT_DATA_FORMAT_SEL = 3'b001
- Register 11[5:4] TDM_WORD_WIDTH = 2'b01 or 2'b00 (24 or 32-bit)
- Register 11[3:2] TDM_BIT_DEPTH = 2'b01 or 2'b00 (24 or 32-bit)
- Register 11[0] TDM_LJ

PCM/TDM Encoder Mapping Registers

- Register 12-13[4:0] TDM_ENC_SLOT_SEL_CH1
- Register 12-13[12:8] TDM_ENC_SLOT_SEL_CH2

DoP Decoder

The ES9292PRO integrates a DoP (DSD over PCM) Decoder that converts the DSD over PCM data into DSD internally following the rest of the internal DSD data path including the DSD Volume, Gain, and Mapping blocks. The channels can be remapped by using the PCM/TDM Decoders Mapping Registers.

DoP Decoder Registers

- Register 2[5] ENABLE_DOP_DECODE = 1'b1
- Register 2[4] ENABLE_TDM_DECODE = 1'b1
- Register 4[3:1] INPUT_DATA_FORMAT_SEL = 3'b001
    - Or Register 4[0] AUTO_INPUT_FORMAT_SEL = 1'b1
- Register 11[5:4] TDM_WORD_WIDTH = 2'b01 or 2'b00 (24 or 32-bit)
- Register 11[3:2] TDM_BIT_DEPTH = 2'b01 or 2'b00 (24 or 32-bit)
- Register 11[0] TDM_LJ

PCM/TDM Decoder Mapping Registers

- Register 13[4:0] TDM_DEC_SLOT_SEL_CH1
- Register 14[4:0] TDM_DEC_SLOT_SEL_CH2

PDM Format

The ES9292PRO features the PDM format with rates from PDM64-PDM512.

Pin Name	Function	Direction	Description
DATA_CLK	PDM CLK	[I/O]	PDM Clock
DATA2	PDM ENC DATA1	[O]	PDM Encoder Channels 1 & 2
DATA4	PDM DEC DATA1	[I]	PDM Decoder Channels 1 & 2

Table 17 - Slave PDM Decoder Pin Connections

Pin Name	Function	Direction	Description
GPIO3	PDM MIC CLK	[O]	PDM Microphone Clock
GPIO4	PDM MIC DATA1	[I]	PDM Microphone Channels 1 & 2

Table 18 - PDM Decoder (Microphone Input) Pin Connections

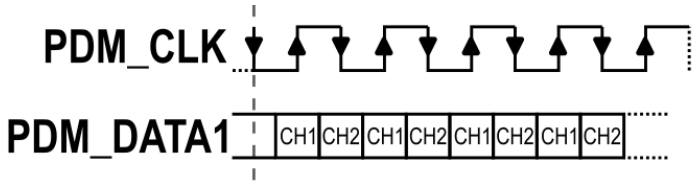


Figure 13 - PDM 2 Channel Format

PDM Encoder

The ES9292PRO integrates a PDM Encoder as an output of the ADC datapath that converts the internal dual channel DSD to PDM data. The Encoders input can be remapped using the DSD Encoder Mapping Registers.

PDM Encoder Registers

- Register 2[2] ENABLE_PDM_ENCODE = 1'b1
- Register 3[3:1] OUTPUT_DATA_FORMAT_SEL = 3'b010
- Register 19[2] PDM_ENC_SAMPLE_EDGE
- Register 19[1] PDM_ ENC _DATA_PHASE
- Register 19[0] PDM_ ENC _2X_GAIN_EN

DSD Encoder Mapping Registers

- Register 18[0] DSD_ENC_CH_SEL_DATA2
- Register 18[1] DSD_ENC_CH_SEL_DATA3

PDM Decoder

The ES9292PRO integrates a PDM Decoder as an input to the DAC datapath that converts the PDM data into dual channel DSD internally to follow the rest of the DSD datapath. The Decoders input can be remapped using the DSD Decoder Mapping Registers.

Note: Register 4[0] AUTO_INPUT_FORMAT_SEL cannot select the PDM format.

PDM Decoder Registers

- Register 2[7] ENABLE_PDM_DECODE = 1'b1
- Register 4[3:1] INPUT_DATA_FORMAT_SEL = 3'b010
- Register 19[6] PDM_DEC_SAMPLE_EDGE
- Register 19[5] PDM_DEC_DATA_PHASE
- Register 19[4] PDM_DEC_2X_GAIN_EN

DSD Decoder Mapping Registers

- Register 18[4] DSD_DEC_LINE_SEL_CH1
- Register 18[5] DSD_DEC_LINE_SEL_CH2

PDM Microphone Decoder (Microphone Input)

The ES9292PRO integrates a Master PDM Microphone Decoder for use as a replacement to the analog input of the ADC. To use the PDM Microphone signal in software mode, PDM_MIC_IN_SEL must be set. PDM Microphone input is also supported in hardware modes, see GPIO Functions in Hardware Mode for more information.

Note: MCLK_PDM_MIC_DIV will follow AUTO_FS_DETECT if enabled and should be set to 7'd3 (default) for a 22.5792MHz/24.576MHz MCLK and 7'd7 for a 45.1584MHz/49.152MHz MCLK to ensure the PDM clock output is 3.072MHz (typical PDM Microphone frequency).

PDM Microphone Decoder Registers

- Register 3[6] ENABLE_PDM_MIC_DECODE = 1'b1
- Register 20[2] PDM_MIC_SAMPLE_EDGE
- Register 20[1] PDM_MIC_DATA_PHASE
- Register 20[0] PDM_MIC_IN_SEL = 1'b1
- Register 20[6:0] MCLK_PDM_MIC_DIV = 7'd3 (default)

S/PDIF Format

The ES9292PRO features the S/PDIF format in the form of a Decoder and an Auxiliary Encoder.

Function	Pin	Direction	Description
S/PDIF ENC OUT	Selected with GPIOx_CFG	[O]	S/PDIF Encoder Output Line
S/PDIF DEC IN	Selected with Reg 24[7:4] SPDIF_DEC_IN_SEL	[I]	S/PDIF Decoder Input Line

Table 19 - S/PDIF Pin Connections

S/PDIF Encoder

The ES9292PRO integrates an Auxiliary S/PDIF Encoder that can be enabled with ENABLE_SPDIF_ENCODE while the PCM/TDM Encoder is running. To do this ensure OUTPUT_DATA_FORMAT_SEL is set to PCM or TDM and set up the respective GPIO as the S/PDIF Encoders output.

The Encoders data source can be chosen between the output of the ADC datapath or the output of the PCM/TDM Decoder with SPDIF_ENC_DATA_SOURCE.

The S/PDIF Encoder includes the ability to customize the 192-bits (24 bytes) of channel status bits one byte at a time by setting SPDIF_ENC_CS_BYTE_ADDR and SPDIF_ENC_CS_BYTE_DATA then toggling SPDIF_ENC_CS_WE to latch the single byte in the status bits. The channel status bits can be passed from the S/PDIF Decoder to the S/PDIF Encoder with the use of SPDIF_ENC_CS_LOOPBACK = 1'b1.

S/PDIF Encoder Registers

- Register 3[7] ENABLE_SPDIF_ENCODE = 1'b1
- Register 3[3:1] OUTPUT_DATA_FORMAT_SEL = 3'b100
    - Or = 3'b000 for Auxiliary
- Register 22[0] SPDIF_ENC_DATA_SOURCE

S/PDIF Channel Status Registers

- Register 22[7] SPDIF_ENC_CS_WE
- Register 22[6] SPDIF_ENC_CS_LOOPBACK
- Register 22[5:1] SPDIF_ENC_CS_BYTE_ADDR
- Register 23 [7:0] SPDIF_ENC_CS_BYTE_DATA

S/PDIF Decoder

The ES9292PRO integrates an S/PDIF Decoder that is coupled closely with a built-in clock Upsampler. The Upsampler generates an internal CLK_UPSMP from the S/PDIF frame. This CLK_UPSMP is then used as the APLL reference clock to generate an MCLK that is synchronous to the S/PDIF frame. See respective section below for more information on the Upsampler and its configurations.

The Channel Status bits can be read one byte at a time using SPDIF_DEC_PAYLOAD_BYTE_SEL and SPDIF_DEC_PAYLOAD_READ. By default, the channel status bits are read from Subframe A and can be changed with SPDIF_DEC_SUBFRAME_READ_SEL.

The validity flag in time slot 28 of the subframe can be ignored with SPDIF_DEC_IGNORE_VALID. The data field in Byte 0[1] of the channel status bits can be ignored when set to “non-audio” with SPDIF_DEC_IGNORE_DATA.

Note: When the ES9292PRO is using the S/PDIF decoder and Upsampler, and an ADC output is desired, the device must be in Master Mode. Master Mode is required to be enabled before the Upsampler is set up. The master mode DCLK divider is set automatically when the Upsampler is running.

S/PDIF Decoder Registers

- Register 4[7] ENABLE_SPDIF_DECODE = 1’b1
- Register 4[3:1] INPUT_DATA_FORMAT_SEL = 3’b100
    - Or Register 4[0] AUTO_INPUT_FORMAT_SEL = 1’b1
- Register 24[0] SPDIF_DEC_IN_SEL
- Register 24[3] SPDIF_DEC_PCM_LOOP
- Register 24[2] SPDIF_DEC_CH_SEL_CH2
- Register 24[1] SPDIF_DEC_CH_SEL_CH1

S/PDIF Channel Status Registers

- Register 25[6] SPDIF_DEC_IGNORE_VALID
- Register 25[5] SPDIF_DEC_IGNORE_DATA
- Register 25[4:0] SPDIF_DEC_PAYLOAD_BYTE_SEL
- Register 26[0] SPDIF_DEC_SUBFRAME_READ_SEL

S/PDIF Decoder Readback Registers

- Register 222 SPDIF_DEC_PAYLOAD_READ

Upsampler

The S/PDIF Decoder is in its own UCLK domain, requiring an external clock input (50MHz recommended & maximum, 38MHz minimum). This clock can be input on either the ACLK1 or ACLK2 pins, chosen by SEL_UCLK_SRC. This UCLK is used by the Upsampler to make the CLK_UPSMP which can be fed into the APLL to generate an MCLK for the rest of theES9292PRO. Ensure Register 126[5:4] SEL_PLL_CLK_IN = 2'b11 (CLK_UPSMP). The CLK_UPSMP frequency is 11.2896/12.288MHz respectively.

S/PDIF Decoder Upsampler Registers

- Register 27[0] SEL_UCLK_SRC
  - Select 1'b1 (50MHz on ACLK2) on ESS Evaluation Boards
- Register 29-30[11:0] UPSMP_UCLK _THRESHOLD
- Register 126[5:4] SEL_PLL_CLK_IN = 2'b11 (CLK_UPSMP).
  - See APLL for more information

UCLK Threshold

The threshold used for the automatic tuning is set by UPSMP_UCLK _THRESHOLD and by default, this threshold is tuned to a 50MHz UCLK. To calculate the threshold for another UCLK rate use the following equation and set Register 29-30[11:0] UPSMP_UCLK _THRESHOLD to the result.

$$\text{Threshold} = 2000 \cdot \frac{\text{UCLK [MHz]}}{\text{50 [MHz]}}$$

DoPoS Format

The ES9292PRO features the DoPoS (DoP over S/PDIF) format by using the DoP Encoder/Decoder in conjunction with the S/PDIF Encoder/Decoder. Since the S/PDIF Encoder and Decoder are the most external interfaces in the DoPoS format they are used for configuration.

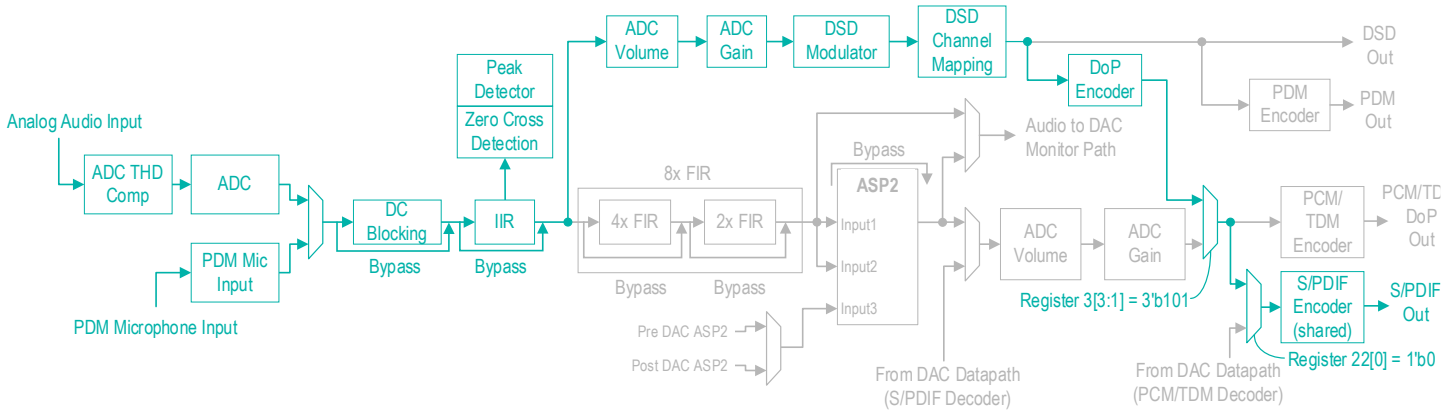
Note: The Auxiliary feature of the S/PDIF encoder does not support the DoPoS format.

Function	Pin	Direction	Description
DoPoS OUT (S/PDIF ENC OUT)	Selected with GPIOx_CFG	[O]	DoPoS (S/PDIF Encoder) Output Line
DoPoS IN (S/PDIF DEC IN)	Selected with Reg 24[7:4] SPDIF_DEC_IN_SEL	[I]	DoPoS (S/PDIF Decoder) Input Line

Figure 14 - DoPoS Pin Connections

DoPoS Encoder

The ES9292PRO integrates a DoPoS Encoder by passing the output of the DoP Encoder to the input of the S/PDIF Encoder. See the below highlighted path for the DoPoS dataflow through the ADC Digital Signal Path.



DoPoS Encoder Registers

- Register 2[2] ENABLE_DOP_ENCODE = 1'b1
- Register 3[7] ENABLE_SPDIF_ENCODE = 1'b1
- Register 3[3:1] OUTPUT_DATA_FORMAT_SEL = 3'b101 (DoPoS)
- Register 22[0] SPDIF_ENC_DATA_SOURCE = 1'b0 (Output of the ADC datapath)

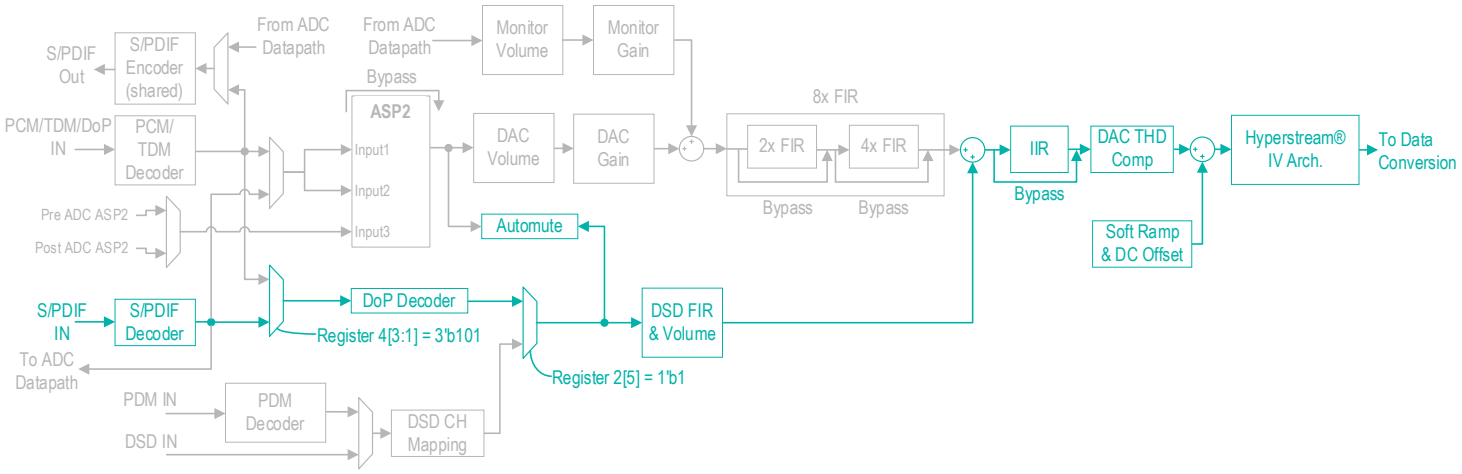
S/PDIF Channel Status Registers

- Register 22[7] SPDIF_ENC_CS_WE
- Register 22[6] SPDIF_ENC_CS_LOOPBACK
- Register 22[5:1] SPDIF_ENC_CS_BYTE_ADDR
- Register 23 [7:0] SPDIF_ENC_CS_BYTE_DATA

DoPoS Decoder

The ES9292PRO integrates a DoPoS Decoder by passing the output of the S/PDIF Decoder to the input of the DoP Decoder. See the below highlighted path for the DoPoS dataflow through the DAC Digital Signal Path.

Note: When the ES9292PRO is using the DoPoS decoder, which requires the Upsampler for the S/PDIF stream, the device must be in PCM Master Mode to create a DCLK for the DoP. Master Mode is required to be enabled before the Upsampler is set up. The master mode DCLK divider is set automatically when the Upsampler is running.



DoPoS Decoder Registers

- Register 2[5] ENABLE_DOP_DECODE = 1'b1
- Register 4[7] ENABLE_SPDIF_DECODE = 1'b1
- Register 4[3:1] INPUT_DATA_FORMAT_SEL = 3'b101 (DoPoS)
- Register 24[0] SPDIF_DEC_IN_SEL
- Register 24[3] SPDIF_DEC_PCM_LOOP = 1'b0 (Doesn't connect S/PDIF decoder output to ADC datapath)
- Register 24[2] SPDIF_DEC_CH_SEL_CH2
- Register 24[1] SPDIF_DEC_CH_SEL_CH1

S/PDIF Channel Status Registers

- Register 25[6] SPDIF_DEC_IGNORE_VALID
- Register 25[5] SPDIF_DEC_IGNORE_DATA
- Register 25[4:0] SPDIF_DEC_PAYLOAD_BYTE_SEL
- Register 26[0] SPDIF_DEC_SUBFRAME_READ_SEL

S/PDIF Decoder Readback Registers

- Register 222 SPDIF_DEC_PAYLOAD_READ

SPI Master Interface

The ES9292PRO features an SPI Master Interface with Zero Cross Detection. The interface is primarily for programming an ASP2 program quickly from a SPI Flash device at high-speed clock rates (up to MCLK/2). The ES9292PRO can use the SPI Master Interface as a generic I²C to SPI Transcoder. This allows the SPI Master to interface with a wide array of devices like flash memories, shift registers, programmable gain amplifiers, and other SPI slave programmable ESS devices. The SPI master interface makes use of the GPIOs in the following table.

GPIO #	SPI Master Function
GPIO4	SS Master 3 (SSM3) or Chip Select Master 3 (CSM3)
GPIO5	SS Master 2 (SSM2) or Chip Select Master 2 (CSM2)
GPIO6	SS Master 1 (SSM1) or Chip Select Master 1 (CSM1)
GPIO7	MISO Master (MISOM)
GPIO8	MOSI Master (MOSIM)
GPIO9	SCLK Master (SCLKM)

Table 20 - SPI Master Interface GPIO Connections

SPI Master Registers

- Register 147 [3] ASP_PROG_SOURCE_SEL should be set low to disconnect the SPI master interface from the ASP2 programming interface.
- Register 198 SPI_MASTER_CONFIG is used to start and end SPI transmissions and set the SPI master clock.
  - [7:4] SPI_M_PULSE_WIDTH – sets the SPI clock frequency
  - [3] SPI_M_EN – Enables the SPI Master interface
  - [2] SPI_M_MODE – Switches the SPI master between Mode 0 (default) and Mode 3
  - [1] SPI_M_SEND_BYTE – Used to manually send/receive SPI bytes.
  - [0] SPI_M_START – Starts and SPI transaction, pulls SSM (GPIO8) low
- Register 199 SPI_MASTER_DATA_OUT – Contains the data byte to be sent from the SPI master interface.
- Register 247-248 [15] SPI_M_ASP_PROG_BUSY – Status of the automated ASP2 Programming
- Register 255 SPI_MASTER_DATA_IN – Contains the data byte received by the SPI master interface.

SPI Write

Writing data on the SPI bus requires 2+n write-register commands where n is the number of bytes to be sent in one SPI transaction. To efficiently write data to an SPI flash Register 198 [1] SPI_M_SEND_BYTE must remain low for automatic SPI data output. Each time Register 199 SPI_M_DATA_OUT is written during an SPI transaction the data will automatically be sent out of the SPI master interface at the end of the write-register command.

A single byte SPI transmission would be sequenced as follows:

1. Setup Register 198 SPI MASTER CONFIG
   - [7:4] SPI_M_PULSE_WIDTH sets the SPI clock speed
   - [3] SPI_M_EN = 1'b1 enables the SPI master
   - [2] SPI_M_MODE selects between SPI modes 0 and 3
   - [1] SPI_M_SEND_BYTE = 1'b0 for automatic operation
   - [0] SPI_M_START prepares the SPI master interface to initiate an SPI transmission.
2. Write a byte of data to Register 199. This will automatically start the SPI transaction.
   - After receiving the write-register command the chip select output (GPIO7) is set low after 2 MCLK cycles.
   - The SPI clock will begin half an SPI clock cycle plus one MCLK cycle after the chip select is set low.
   - The SPI master interface will output the 8 bits of data and afterwards the SPI clock will remain idle, and the chip select low.
3. Resetting Register 198 [0] SPI_M_START low will end the SPI transaction by setting the chip select high.

To write multiple bytes of data in one SPI transaction repeat step 2 for each byte. As an example, the following sequence will write a 16-bit value to a specified address in the SPI Flash to be used as a version identifier for an ASP program.

```
void I²C_WriteFlash(uint32_t addr, uint16_t data)
{
  I²C_WriteReg(198, 0x19);  // Start SPI
  I²C_WriteReg(199, 0x06);  // Write Enable Command
  I²C_WriteReg(198, 0x18);  // End SPI

  I²C_WriteReg(198, 0x19);  // Start SPI
  I²C_WriteReg(199, 0x02);  // Page Program Command

  I²C_WriteReg(199, addr >> 16);  // 24-bit Address
  I²C_WriteReg(199, addr >> 8);
  I²C_WriteReg(199, addr);

  I²C_WriteReg(199, data >> 8);  // 16-bit Data
  I²C_WriteReg(199, data);

  I²C_WriteReg(198, 0x18);  // End SPI
}
```

SPI Read

The data byte received on the SPI master interface is stored in Register 255 SPI_MASTER_DATA_IN. The last byte of data stored can be read back at any time with a read-register command. Sequential SPI reads can be efficiently performed by automatically triggering after each read-register command while the Register 198 [1] SPI_M_SEND_BYTE bit remains low. In this configuration when Register 255 is readback the data currently in it will be transmitted on the I²C or SPI slave interfaces and immediately after the read-register command finishes the SPI master interface will automatically trigger another sequence of 8 bits to load in the next byte of data. During a read-register command whatever data is already stored in Register 199 SPI_MASTER_DATA_OUT will be output again for each read-register command on Register 255.

The following example sequence reads a 16-bit value from a specified address in an SPI Flash.

```
uint16_t I²C_ReadFlash(uint32_t addr)
{
  I²C_WriteReg(198, 0x19);  // Start SPI
  I²C_WriteReg(199, 0x03);  // Read Data Command

  I²C_WriteReg(199, addr >> 16);  // 24-bit Address
  I²C_WriteReg(199, addr >> 8);
  I²C_WriteReg(199, addr);

  I²C_WriteReg(199, 0x00);       // Dummy data to load in first byte from SPI Flash
  uint8_t x1 = I²C_ReadReg(255); // Reads first byte from ES98x3QPRO and then loads second byte form SPI Flash
  I²C_WriteReg(198, 0x18);       // End SPI
  uint8_t x2 = I²C_ReadReg(255); // Reads second byte from ES9841

  return (x1 << 8 | x2);  // Return 16-bit data
}
```

SPI Simultaneous Read and Write

In the default automatic mode, it is not possible to write new data while the data is being read back on the I²C or SPI slave interfaces. This is not an issue with the SPI flash chips which the SPI master interface is intended to be used with. However, there is way to sequence the commands to be able to both read and write data at the same time without the automatic sequencing:

1. While the SPI master is not currently active, load the first byte of data into Register 199
2. Enable the SPI output with Register 198 and set bit [1] high to begin the SPI transaction and output the first byte of data
3. While Register 198 [1] remains high, the first data byte received can be readback (Register 255) without automatically triggering another byte sequence
4. The second byte of data to be transmitted can then be loaded into Register 199, again without automatically triggering a byte sequence.
5. Then Register 198 [1] must be set low and back high again to trigger the next SPI sequence. The sequence will immediately follow the write-register command setting that bit high.
6. Afterwards the data received can be readback from Register 255 and the next byte loaded into Register 199 again.
7. To end the SPI transaction set Register 198 [0] low and the chip select will immediately be set high.

As long as Register 198 [1] is high, data can be written and read from the SPI master interface without automatically triggering the SPI master output. Any time the bit is set high the SPI master interface will output the data currently in Register 199 and replace the data in readback Register 255. This process to manually read and write takes four read/write register commands for each byte of data to be transmitted on the SPI master interface.

```
I²C_WriteReg(199, 0x03); // Load first data byte
I²C_WriteReg(198, 0x1B); // Start SPI
I²C_ReadReg(255);        // Read first data byte

I²C_WriteReg(199, 0x12); // Load second data byte
I²C_WriteReg(198, 0x19); // Toggle Send Byte bit
I²C_WriteReg(198, 0x1B);
I²C_ReadReg(255);        // Read second data byte

I²C_WriteReg(198, 0x18); // End SPI
```

SPI Serial Flash Control & Shift Register Control

The ES9292PROs SPI Master Interface can interact with a multitude of SPI Devices such as Serial Flash Controls and Shift Registers.

SPI Serial Flash can be used to store the programmable instructions and coefficients for the ASP2. The programming will change depending on the specific architecture of the SPI flash and the MCU used to send the instructions. For an application note on the ASP2, please ask your FAE or Distributor for availability.

The SPI Master Interface can also be used to interact with shift registers, effectively adding a serial to parallel converter to the ES9292PRO.

For more information on the SPI Master Interface and its applications please ask your FAE or Distributor for the Application Note.

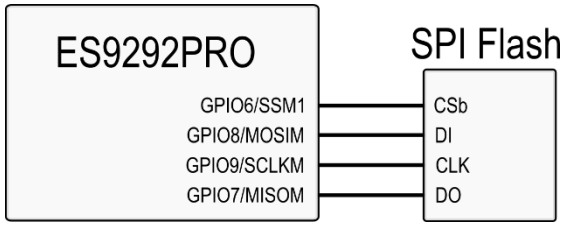


Figure 15 - Example SPI Flash Schematic

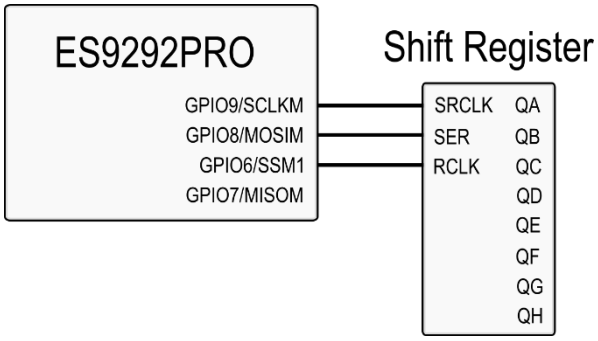


Figure 16 - Example SPI Shift Register Schematic

ASP2 (Audio Signal Processor)

The SMART CODEC incorporates ESS Technology's 2nd generation Audio Signal Processors (ASP2) on both the ADC/DAC data paths. These features allow customers to target their audio requirements, by optionally integrating multi-band PEQs, MIXERs, Audio Expanders and Compressors (DRC), AGL, stereo widening, SABREXBASS enhancement and other specialty filters optimized with AI tools. ESS' SABRE Intelligence Studio (SI Studio) GUI with AI capability reduces programming complexity of the ASP2 and reduces or eliminates customer DSP requirements.

The ASP2 can be programmed using the slave I²C/SPI interface or with the SPI master interface with an external SPI flash memory as shown in SPI Serial Flash Control & Shift Register Control.

There is an ASP2 core per channel, per datapath, for a total of 4 ASP2 cores in the ES9292PRO. Each datapath's cores share the same program RAM (PRAM) and have individual coefficient RAM and data RAM. This application note describes the architecture of the ASP2 in the ES9292PRO to allow users to better understand the limitations when designing ASP2 programs with the ESS Suite's SI Studio interface.

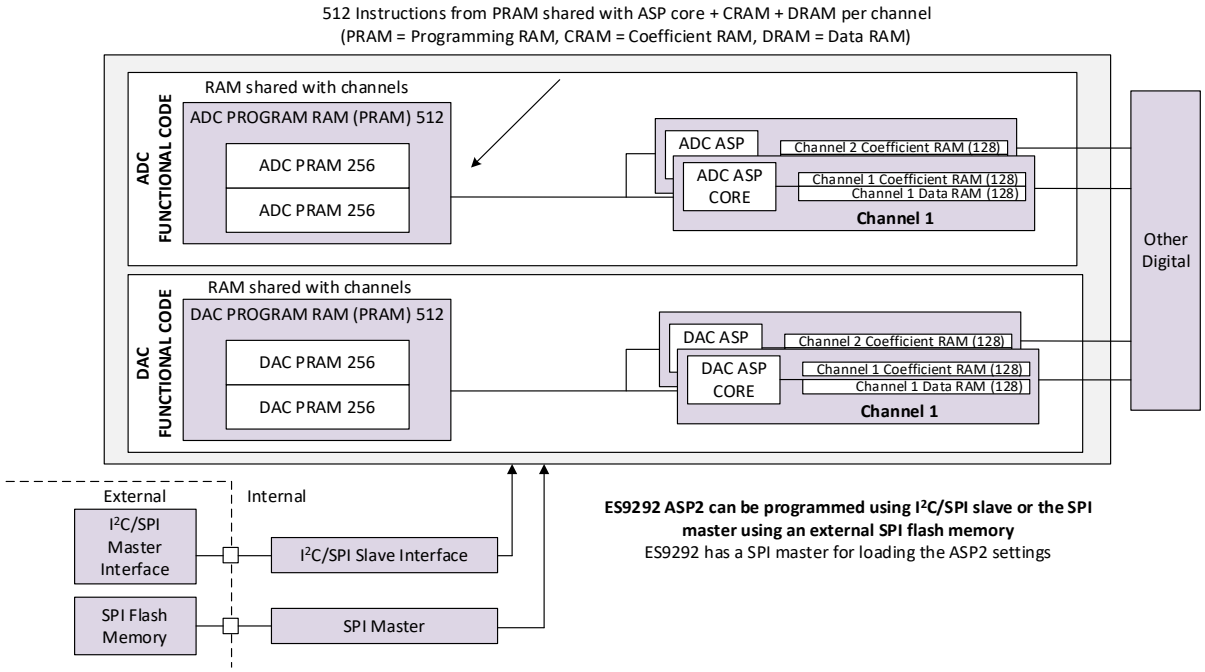


Figure 17 - ES9292PRO ASP2 Overview

The ASP2 can be programmed to represent (among others):

- High-efficiency IIR/Biquad filters
- Mixers
- Parametric Equalizers (PEQ), including 25 band PEQs
- Multi-band Dynamic Range Compression (DRC) operations
- Automatic Gain Limiters (AGL)
- Specialty filters including Crossovers & RIAA Equalization pre/de-emphasis filters
- Stereo Widening
- Audio Expansion and Compression
- SABREXBASS enhancement

The integration of the ASP2 into the datapath alleviates processing requirements on the system processor and helps simplify system design.

For more information on the ASP2 or SI Studio tool, please contact your local ESS FAE or distributor for availability.

Advanced Mixing

In addition, the ES9292PRO allows for inter-path mixing by using the ASP2's Input3. Each path (ADC and DAC) can mix their audio into the other path's ASP2 by using the Pre or Post ASP2 mix point as an input. This allows for advanced mixing between the ADC and DAC paths.

In addition to cross path mixing, Input3 can input status flags from GPIOs by setting ASP_(ADC/DAC)_IN3_SEL_CHx = 1'b1. The respective GPIO must be free to use, ie not currently in use by any encoder, decoder, or transcoder.

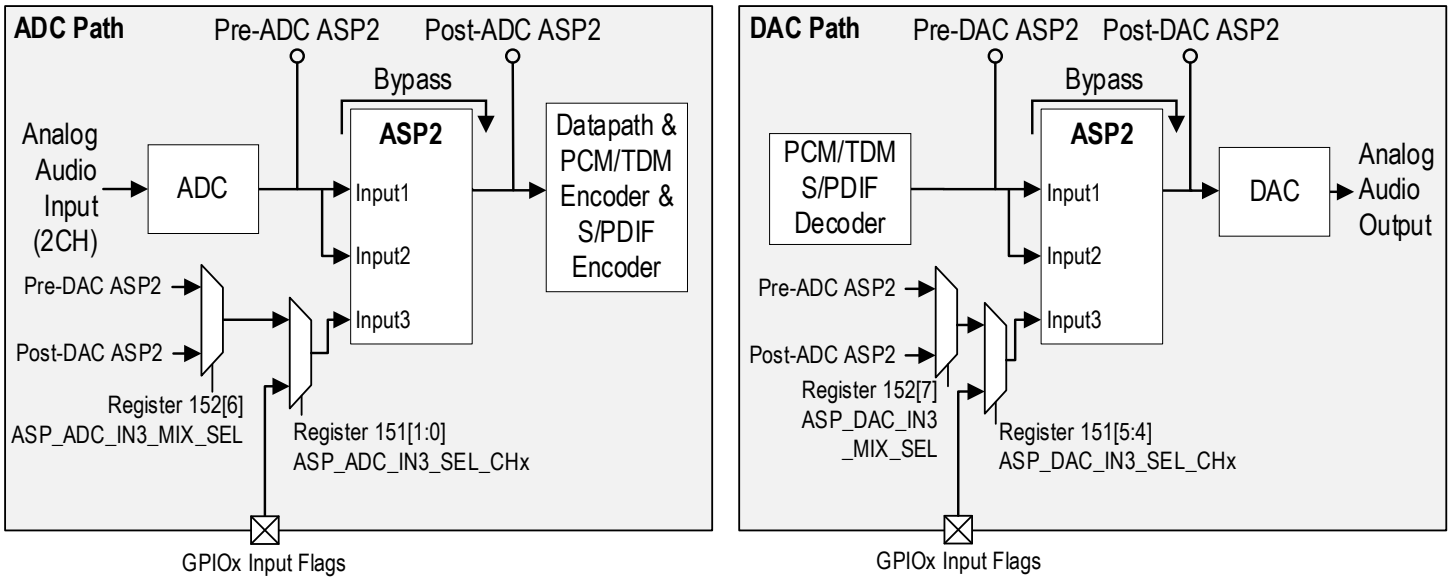
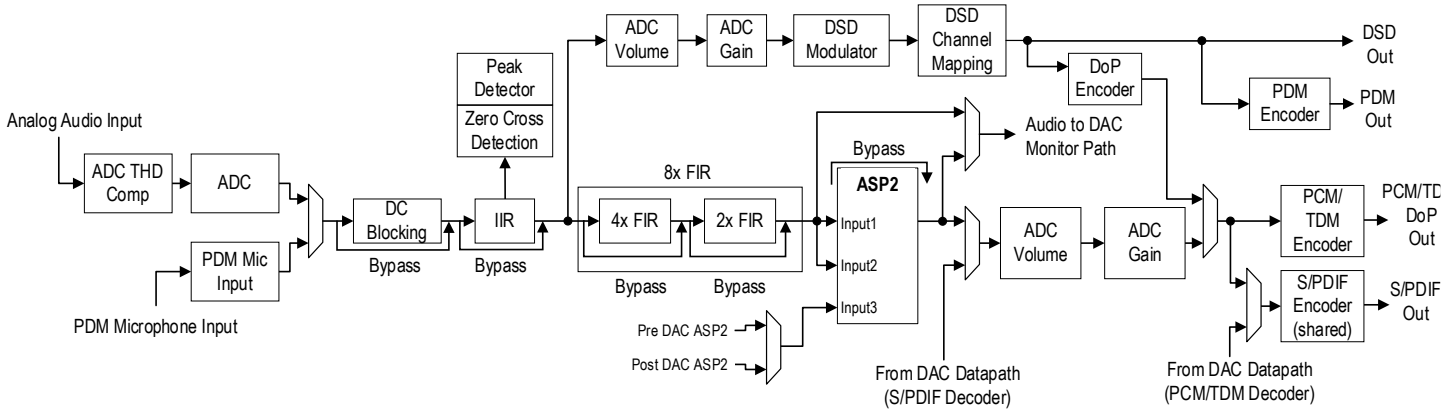


Figure 18 - ES9292PRO ASP2 Advanced Mixing

Advanced Mixing Registers

- Register 151[5:4] ASP_DAC_IN3_SEL_CHx
- Register 151[1:0] ASP_ADC_IN3_SEL_CHx
- Register 152[7] ASP_DAC_IN3_MIX_SEL
- Register 152[6] ASP_ADC_IN3_MIX_SEL

ADC Digital Signal Path



DC Blocking

The integrated DC Blocking filter exhibits a high cutoff frequency (-3dB @ 0.25Hz).

DC Blocking Registers

- Register 84-83[13, 14] DC_BLOCK_EN_CHx

ADC IIR

The IIR filter can be bypassed using Register 82[2:0] ADC_BYPASS_IIR

ADC 8x FIR

Selection of the 8x Interpolation filter can be chosen from 8 pre-programmed filter shapes or programmed with custom coefficients. The 2x and 4x filter can be bypassed individually or together. For more information on the preset filters see Pre-Programmed Digital Filters. For more information on the programmable ADC FIR please ask your FAE or distributor for the Programmable FIR Application Note.

ADC 8x FIR Registers

- Register 82[7:5] ADC_FILTER_SHAPE
- Register 82[4] ADC_BYPASS_FIR2X
- Register 82[3] ADC_BYPASS_FIR4X

ADC Programmable FIR Registers

- Register 84-83[11] ADC_PROG_FIR_COEFF_WE
- Register 84-83[10] ADC_PROG_FIR_COEFF_EN
- Register 85[7] ADC_PROG_FIR_COEFF_STAGE
- Register 85[6:0] ADC_PROG_FIR_COEFF_ADDR
- Register 88-86 ADC_PROG_FIR_COEFF_IN

Peak Detector

Peak Detector Enable Registers

- Register 97[0,1] PEAK_DETECT_EN_CHx

Peak Flag GPIO Registers

- Register 76[1:0] ADC_CH1_DET_FLAG_SEL = 1'b0
- Register 76[3:2] ADC_CH2_DET_FLAG_SEL = 1'b0
- Register 42[0, 1] MASK_PEAK_DET_CHx
- Register 43[0, 1] CLEAR_PEAK_DET_CHx

Peak Flag Latching and Readback Registers

- Register 98[6] LOCK_PEAK_VALUE
- Register 232 [2, 3] PEAK_FLAG_LAT_CHx
- Register 232[0, 1] PEAK_FLAG_CHx
- Register 237-234 PEAK_LEVEL_CHx

Peak Flag Decay Rate and Threshold Registers

- Register 98[4:0] PEAK_DECAY_RATE
- Register 100-99 PEAK_THRESH_CHx

ADC Volume

The ADC Volume Control is intended for use during audio playback. Each channel can be digitally attenuated from +1dB to -126dB in 0.5dB steps. When a new volume level is set, the attenuation circuit will ramp softly to the new level at a rate specified in the VOLUME RAMP RATE UP and VOLUME RAMP RATE DOWN registers.

ADC Volume Registers

- Register 90-89[15:8] ADC_VOLUME_CH1
- Register 90-89[7:0] ADC_VOLUME_CH2
- Register 37-36[15:8] VOLUME_RAMP_RATE_DOWN
- Register 37-36[7:0] VOLUME_RAMP_RATE_UP
- Register 38[0] VOL_RAMP_SPEED_SEL

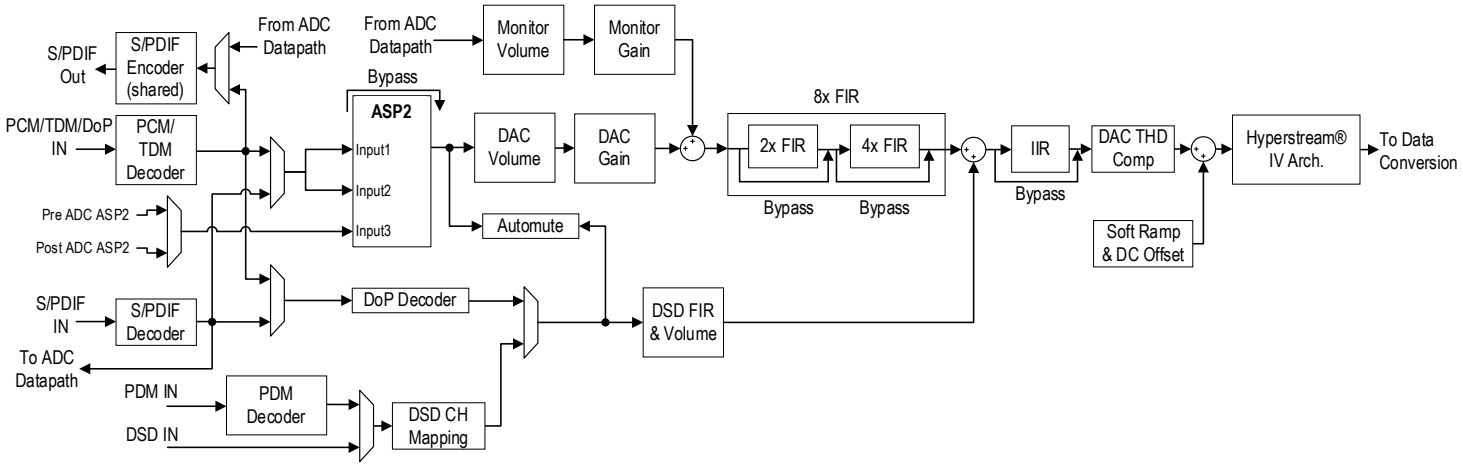
ADC Gain

The ES9292PRO has an additional digital gain that can be added through registers. Settings for +0dB to +42dB in +6dB steps are available.

ADC Gain Registers

- Register 91[6:4] ADC_DIGITAL_GAIN_CH2
- Register 91[2:0] ADC_DIGITAL_GAIN_CH1

DAC Digital Signal Path



DAC Gain

The ES9292PRO has an additional digital gain that can be added through registers. Settings for +0dB to +42dB in 6dB steps are available.

DAC Gain Registers

- Register 114[6:4] DAC_DIGITAL_GAIN_CH2
- Register 114[2:0] DAC_DIGITAL_GAIN_CH1

DAC Volume

The DAC Volume Control is intended for use during audio playback. Each channel can be digitally attenuated from -126dB to +1dB in +0.5dB steps. When a new volume level is set, the attenuation circuit will ramp softly to the new level at a rate specified in the VOLUME UP RAMP RATE and VOLUME DOWN RAMP RATE registers.

DAC Volume Registers

- Register 110-111[7:0] DAC_VOLUME_CH1
- Register 110-111[15:8] DAC_VOLUME_CH2
- Register 36-37[7:0] VOLUME_UP_RAMP_RATE
- Register 36-37[15:8] VOLUME_DOWN_RAMP_RATE
- Register 38[0] VOL_RAMP_SPEED_SEL

Automute

The DAC in the ES9292PRO features an automute that triggers when the signal is below the specified level for longer than the specified time. The automute will disengage when the signal is above the specified off value for the same amount of time.

In HW Mode Automute is controlled by the state of the HW4 pin (Pin 41), the pin must be in the “Pull 1” or “1” state to enable Automute. The Automute thresholds and times in HW mode follow the default SW mode values.

In SW mode Automute is enabled by default and can be disabled on each channel individually through Register 120 AUTOMUTE_ENABLE.

When Automute engages, the DAC Volume block will lower the volume until it’s muted according to VOL_RATE_DOWN. When it disengages it will raise the volume back to normal according to VOL_RATE_UP. During an abnormal mute condition (an invalid BCK/WS ratio) it will lower the volume at the maximum rate (8’hFF). For more information on those registers see the DAC Volume section.

The thresholds that engage and disengage Automute can be configured through the AUTOMUTE_LEVEL and AUTOMUTE_OFF_LEVEL registers. Automute will engage or disengage when any one of the following conditions are met.

Mode	Detection Condition
PCM	• Data is lower than AUTOMUTE_LEVEL for longer than the Automute Time. • Data is at a constant DC level for longer than Automute Time.
DoP/DSD	• DSD data contains a DSD mute pattern (equal number of 1’s and 0’s in 8 consecutive bits of data), for longer than Automute Time. • DSD data contains all 1’s or 0’s in 8 consecutive bits of data, for longer than Automute Time.

Note: Automute will not engage if the Direct Monitor is running.

$$Time[s] = \frac{2^{18}}{AUTOMUTE\_TIME * FS}$$

$$Level[dB] = \frac{20 * log_{10}(AUTOMUTE\_LEVEL)}{(2^{16} - 1) * 2^{7}}$$

Automute Configuration Registers

- Register 120: AUTOMUTE_ENABLE
- Register 121-122[10:0]: AUTOMUTE_TIME
- Register 123-126[15:0]: AUTOMUTE_LEVEL
- Register 123-126[16:21]: AUTOMUTE_OFF_LEVEL
- Register 121-122[15] DSD_FAULT_DET_EN - Sets data to a DSD mute pattern (0x96) if the DSD data has no changes in 64 DATA_CLKs.
- Register 121-122[14]: DSD_DC_AM_EN - Enables the DSD automute condition for 8 consecutive bits of 1’b1 or 1’b0
- Register 121-122[13]: DSD_MUTE_AM_EN - Enables the DSD automute condition for the DSD Mute pattern

See next page for example diagrams of Automute Engaging and Disengaging, with and without Mute Ramp to Ground enabled. See Soft Ramp & DC Offset for more information Mute Ramp to Ground.

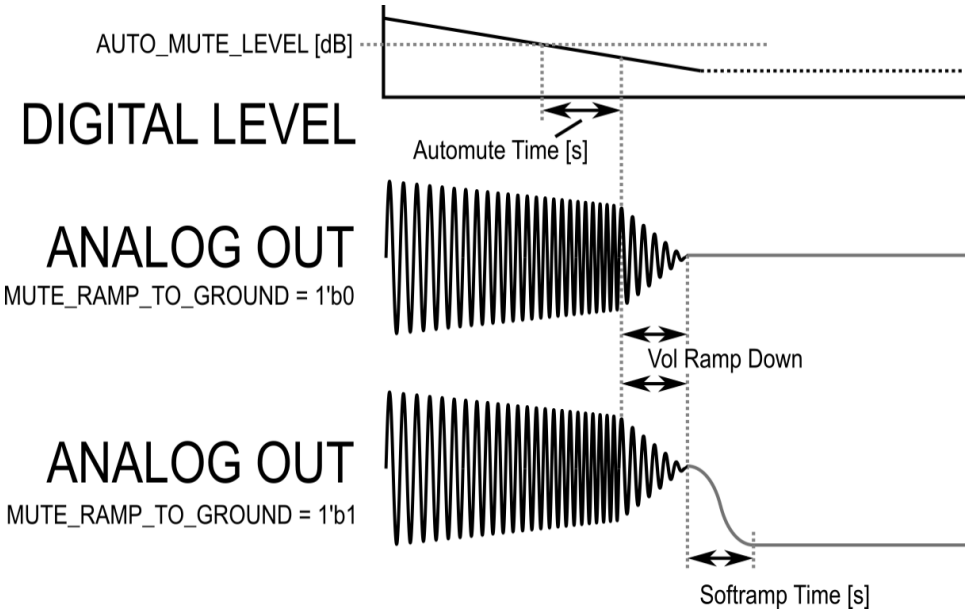


Figure 19 - Automute Engaging

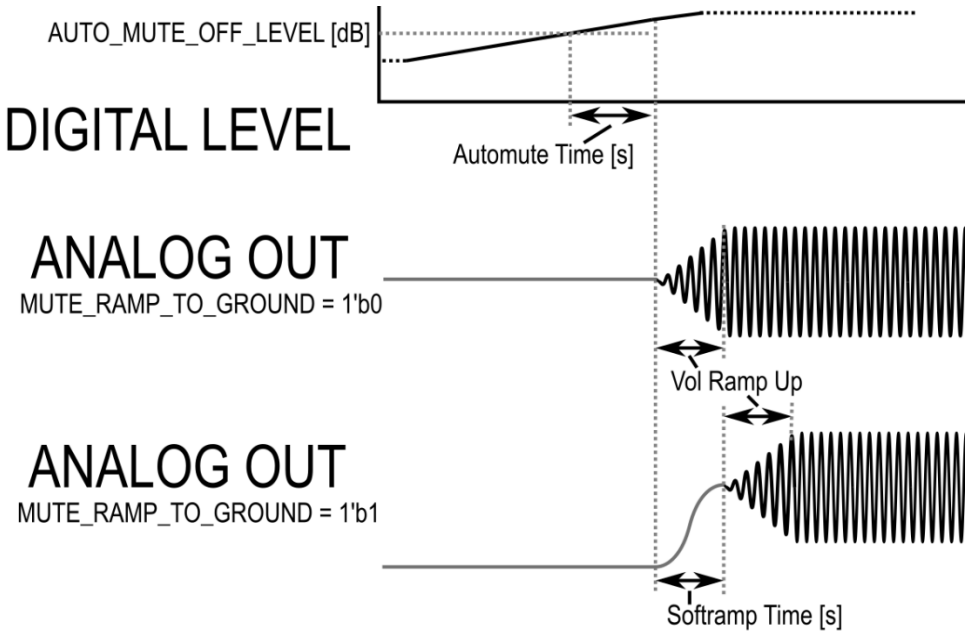


Figure 20 - Automute Disengaging

DAC 8x FIR

Selection of the 8x interpolation filter is chosen from 8 pre-programmed filters or programmed with custom coefficients. The 2x and 4x filter can be bypassed individually or together. For more information on filters see the Pre-Programmed Digital Filters section. For more information on the programmable DAC FIR please ask your FAE or distributor for the Programmable FIR Application Note.

DAC FIR Registers

- Register 105[2:0] DAC_FILTER_SHAPE
- Register 105[3] BYPASS_FIR2X
- Register 105[4] BYPASS_FIR4X

DAC Programmable FIR Registers

- Register 105[7] DAC_PROG_FIR_COEFF_WE
- Register 105[6] DAC_PROG_FIR_COEFF_EN
- Register 106[7] DAC_PROG_FIR_COEFF_STAGE
- Register 106[6:0] DAC_PROG_FIR_COEFF_ADDR
- Register 109-107 DAC_PROG_FIR_COEFF_IN

DAC IIR

The IIR filter can be bypassed using Register 105[5] BYPASS_IIR

Soft Ramp & DC Offset

The ES9292PRO saves power by ramping to ground during a normal mute condition. This includes automute, register mute, and GPIO mute.

A DC offset can be added to each datapath signal in 100uV increments.

Note: The Soft Ramp Time has a maximum value of 4'd15.

Soft Ramp & DC Offset Registers

- Register 117[5] MUTE_RAMP_TO_GROUND
- Register 117[4:0] SOFT_RAMP_TIME
- Register 118-119 DC OFFSET

$$\text{Soft Ramp Time [s]} = \frac{2^{16} \cdot 2^{\text{SOFT\_RAMP\_TIME}}}{MCLK \cdot 2^{\sim\text{MCLK\_24M\_DIV2}}}$$

Direct Monitor Volume

Signals from the ADC digital path can be passed into the DAC digital path using the Direct Monitor, either individually to their respective channels or in a mono configuration where both ADC channels will be passed to the DAC channel. The audio will be taken from either the Pre or Post ASP path indicated in the DAC Digital Signal Path, configured with DIR_MON_ADC_SEL.

The Direct Monitor Volume Control is intended for use during audio playback. Each channel can be digitally attenuated from +1dB to -126dB in 0.5dB steps. When a new volume level is set, the attenuation circuit will ramp softly to the new level at a rate specified in the VOLUME UP RAMP RATE and VOLUME DOWN RAMP RATE registers.

Monitor Volume Registers

- Register 112-113 DIRECT MONITOR VOLUME
- Register 115[5:4] DIR_MON_MONO_CHx
- Register 115[3:2] DIR_MON_VOL_PHASE_INV_CHx
- Register 116[5:4] DIR_MON_MUTE_CHx
- Register 117[6] DIR_MON_ADC_SEL

Note: Using the Direct Monitor will disable Automute functionality.

Direct Monitor Gain

The Direct Monitor uses the same gain settings as the ADC Gain does.

Monitor Gain Registers

- Register 91[6:4] ADC_DIGITAL_GAIN_CH2
- Register 91[2:0] ADC_DIGITAL_GAIN_CH1

GPIO Configuration

GPIO_CONFIG	Function	I/O Direction
0	Analog Outputs Off	Shutdown
1	Mute DAC Channels	Input
2	Clock Valid Flag	Output
3	PLL Locked Flag	Output
4	DAC Minimum Volume Flag	Output
5	DAC Automute Status Flag	Output
6	DAC Soft Ramp Done Flag	Output
7	ADC CH1 Flags	Output
8	ADC CH2 Flags	Output
9	OR of Status Bits	Output
10	S/PDIF Encoder Stream	Output
11	PWM Signal	Output
12	Output 0	Output
13	ASP Status Flags	Input/Output
14-15	Reserved	-

GPIOx Default States:

GPIO1-9: Analog Outputs Off

Analog Outputs Off

The GPIO is shutdown and has no functionality.

Mute DAC Channels

Mute both DAC channels and Direct Monitor.

Clock Valid Flag

Outputs HIGH if a MCLK source is detected. Outputs LOW when clock is removed or not present.

Relevant Registers

- Register 8[0] CLK_FAULT_DET_EN must be asserted for the clock valid flag to operate.

PLL Locked Flag

Outputs HIGH if the PLL is locked.

Relevant Registers

- Register 8[1] FORCE_PLL_LOCK must be 1'b0 to see the status of the PLL, else this flag will output HIGH.

DAC Minimum Volume Flag

Outputs HIGH when the DAC is muted. This can occur from manual muting, automuting, and setting volume to 0xFF.

Relevant Registers

- Register 77[0] GPIO_AND_VOL_MIN sets the output to be the logical AND of both channels' mute flags.
- Register 77[3] GPIO_OR_VOL_MIN sets the output to be the logical OR of both channels' mute flags.
- Register 77[6] DAC_FLAG_CH_SEL selects which of the individual DAC channel flags to output.

DAC Automute Status Flag

Outputs HIGH when the DACs automute condition is met.

Relevant Registers

- Register 77[1] GPIO_AND_AUTOMUTE sets the output to be the logical AND of both channels' automute flags.
- Register 77[4] GPIO_OR_AUTOMUTE sets the output to be the logical OR of both channels' automute flags.
- Register 77[6] DAC_FLAG_CH_SEL selects which of the DAC channel flags to output.

DAC Soft Ramp Done Flag

Outputs HIGH when the DAC is neither ramping up nor down.

Relevant Registers

- Register 77[2] GPIO_AND_SS_RAMP sets the output to be the logical AND of both channels' automute flags.
- Register 77[5] GPIO_OR_SS_RAMP sets the output to be the logical OR of both channels' automute flags.
- Register 77[6] DAC_FLAG_CH_SEL selects which of the DAC channel flags to output.

ADC CH1/2 Flags

ADC CH1/2 detection flag output can be set to the Peak Detector Flag, ADC Overload Flag, or Zero Cross. The live or latched version of the flags can be output. By default, the latched peak detect flag is output.

Relevant Registers

- Register 76[4] ADC_LIVE_FLAG_SEL determines live or latched flag output
- Register 76[3:2. 1:0] ADC_CHx_DET_FLAG_SEL
    - 2'd0: Peak Detect Flag (default)
    - 2'd1: ADC Overload Flag
    - 2'd3: Zero-Cross Detect
    - 2'd4: Reserved

OR of Status Bits

Outputs the bitwise OR of all masked status bits. This includes the DAC and ADCs Zero-Cross detect flags, as well as the ADCs Overload and Peak Detector Flags.

Relevant Registers

- Register 42 STATUS BITS MASK
- Register 43 STATUS BITS CLEAR

S/PDIF Encoder Stream

Outputs the S/PDIF Stream from the S/PDIF Encoder.

PWM Signal

Outputs a configurable PWM signal. The frequency and duty cycle of the PWM signal can be calculated with the following equations:

$$frequency\ [Hz] = \frac{MCLK}{PWM\_FREQ + 1}$$

$$Duty\ Cycle\ [\%] = \left(\frac{PWM\_COUNT}{PWM\_FREQ + 1}\right) \times 100$$

Relevant Registers

- Register 78 PWM_COUNT
- Register 79-80 PWM_FREQ

Output 0

Outputs a constant 1'b0. Invert to output a constant 1'b1.

ASP Status Flags

Connects the GPIO to the ASP2 Core for use in the ASP2 program.

If the respective GPIOx_IE = 1'b1, the GPIO will be connected to the ASP2 cores Input3 with a per-core mux controlling whether the core receives the GPIO inputs or the TDM decoder signal. The mux is controlled with Register 151[5:4, 1:0] ASP_(DAC/ADC)_IN3_SEL_CHx.

If the respective GPIOx_OE=1'b1, the GPIO will be connected to the ASP2 core, allowing flags set by the ASP2 program to be read externally.

Pre-Programmed Digital Filters

The ES9292PRO has 8 pre-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates. (See Register 82[7:5] ADC_FILTER_SHAPE and Register 105[2:0] DAC_FILTER_SHAPE for configuration)

#	Filter	Description
1	Minimum Phase (default)	Version 2 of minimum phase fast roll-off (#6) with less ripple and more image rejection
2	Linear Phase Apodizing Fast Roll-Off	Full image rejection by FS/2 to avoid any aliasing, with smooth roll-off starting before 20k.
3	Linear Phase Fast Roll-Off	Sabre legacy filter, optimized for image rejection @ 0.55FS
4	Linear Phase Fast Roll-Off Low-Ripple	Sabre legacy filter, optimized for in-band ripple
5	Linear Phase Slow Roll-Off	Sabre legacy filter, optimized for lower latency, but symmetric impulse response
6	Minimum Phase Fast Roll-Off	Low latency, minimal pre ringing and low passband ripple, image rejection @ 0.55FS
7	Minimum Phase Slow Roll-Off	Lowest latency at the cost of image rejection
8	Minimum Phase Fast Roll-Off Low Dispersion	Provides a nice balance of the low latency of minimum phase filters and the low dispersion of linear phase filters. Minimal pre-ringing is added to achieve the low dispersion in the audio band.

Table 21 - Pre-Programmed Digital Filter Descriptions

Note: Minimum phase filters are asymmetric filters that work to minimize the pre-echo of the filter, while still maintaining an excellent frequency response and they peak earlier than linear phase filters, resulting in a lower group delay. Minimum phase filters usually feature zero cycles of pre-echo, which can result in improved audio quality.

ADC: PCM Filter Latency

The following table shows the simulated latency of each filter across different sampling rates. Measurements were taken from the external impulse response prior to being down sampled to 1FS. The extra sample delay due to data encoding accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

Filter Shape \ Frequency [kHz]	44.1 / 48	88.2 / 96	176.4 / 192	352.8 / 384
Minimum Phase (default)	5.36 / FS	5.47 / FS	5.69 / FS	6.25 / FS
Linear Phase Apodizing Fast Roll-Off	35.23 / FS	35.34 / FS	35.63 / FS	36.12 / FS
Linear Phase Fast Roll-Off	35.36 / FS	35.47 / FS	35.75 / FS	36.25 / FS
Linear Phase Fast Roll-Off Low-Ripple	34.98 / FS	35.09 / FS	35.38 / FS	36.00 / FS
Linear Phase Slow Roll-Off	7.86 / FS	8.09 / FS	8.38 / FS	9.00 / FS
Minimum Phase Fast Roll-Off	5.48 / FS	5.59/ FS	5.88 / FS	6.37 / FS
Minimum Phase Slow Roll-Off	4.35 / FS	4.47/ FS	4.69 / FS	5.25 / FS
Minimum Phase Slow Roll-Off Low Dispersion	6.23 / FS	6.34 / FS	6.56 / FS	7.25 / FS

Table 22 - ADC PCM Filter Latency

ADC: PCM Filter Properties

Minimum Phase					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-100.4 dB	0.55 FS			Hz
Group Delay		2.90/FS		9.23/FS	s
Flatness (ripple)	0.0030				dB

Linear Phase Apodizing					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.41 FS	Hz
Stop band	-108.9 dB	0.50 FS			Hz
Group Delay			33.25/FS		s
Flatness (ripple)	0.0033				dB

Linear Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-115.5 dB	0.55 FS			Hz
Group Delay			33.38/FS		s
Flatness (ripple)	0.0038				dB

Linear Phase Fast Roll-Off Low Ripple					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-82.53 dB	0.55 FS			Hz
Group Delay			33/FS		s
Flatness (ripple)	0.0021				dB

Linear Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.46 FS	Hz
Stop band	-85.02 dB	0.75 FS			Hz
Group Delay			6.05/FS		s
Flatness (ripple)					dB

Minimum Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-101.2 dB	0.55 FS			Hz
Group Delay		2.95/FS		9.42/FS	s
Flatness (ripple)	0.0048				dB

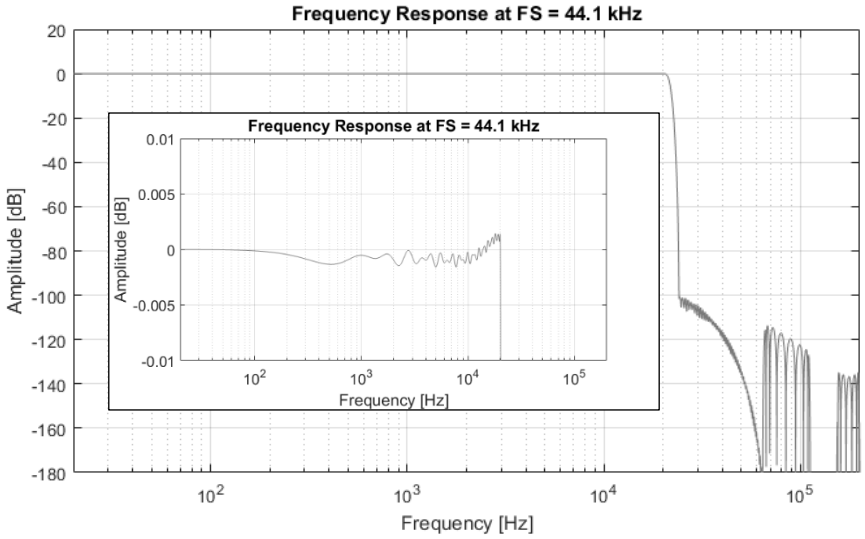
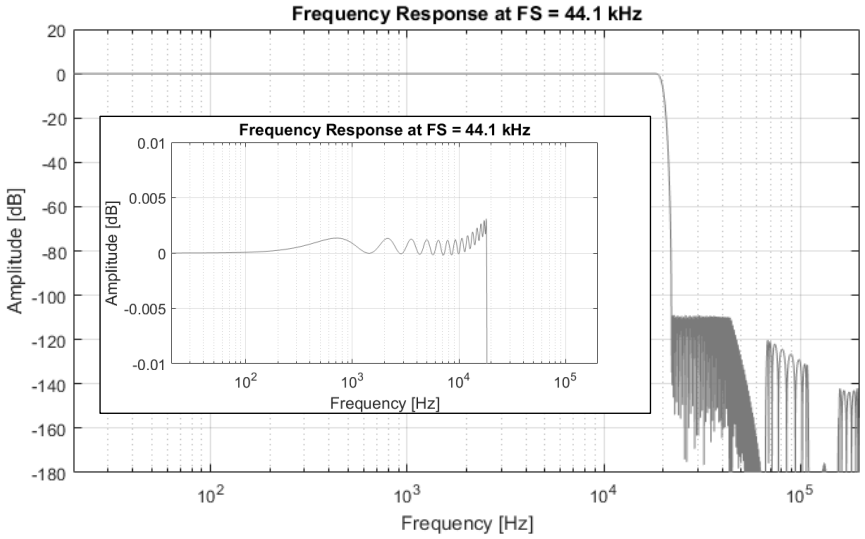
Minimum Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.43 FS	Hz
Stop band	-90.34 dB	0.80 FS			Hz
Group Delay		2.03/FS		3.51/FS	s
Flatness (ripple)					dB

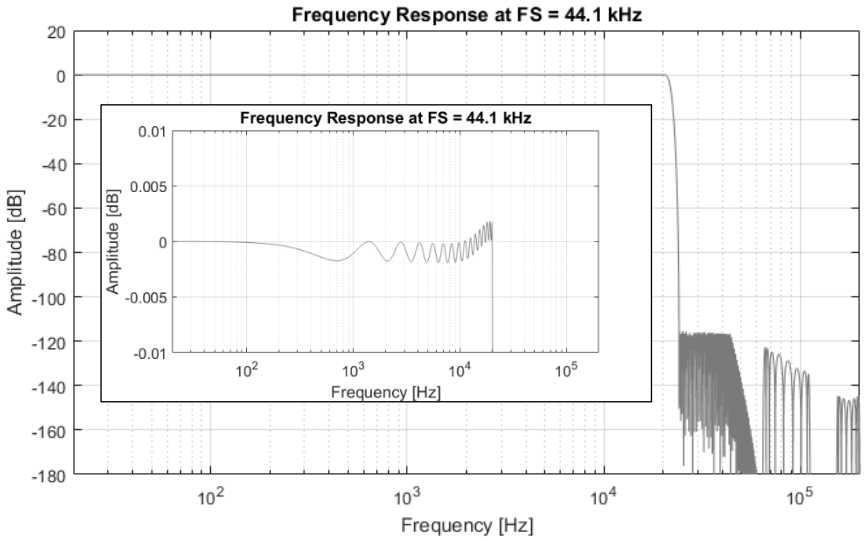
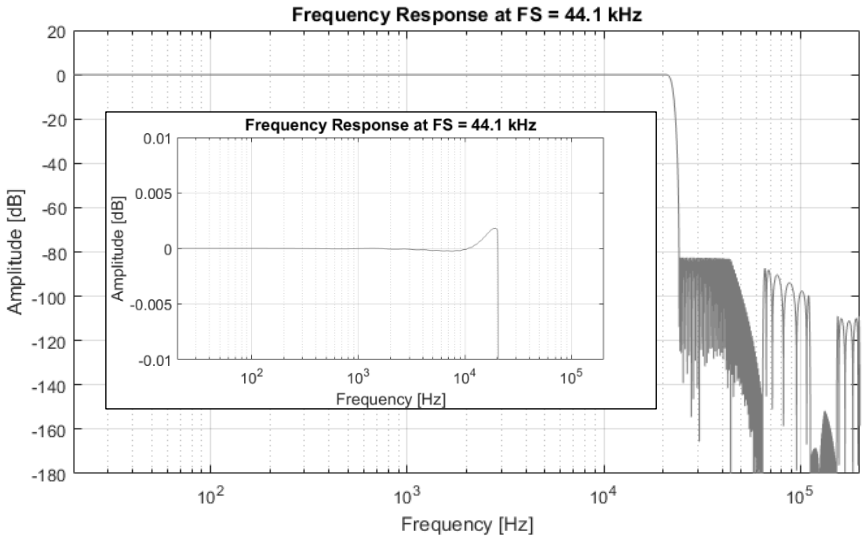
Minimum Phase Slow Roll-Off Low Dispersion					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.45 FS	Hz
Stop band	-98.8 dB	0.82 FS			Hz
Group Delay		4.12/FS		4.38/FS	s
Flatness (ripple)					dB

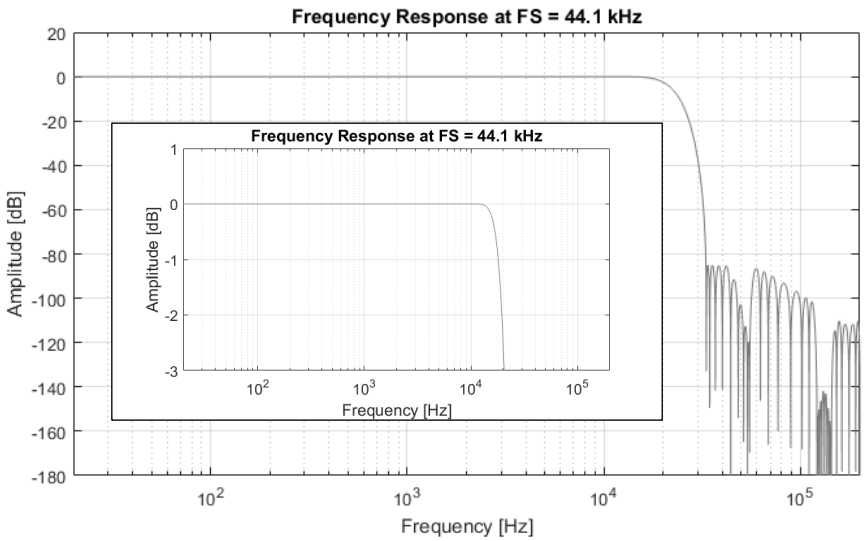
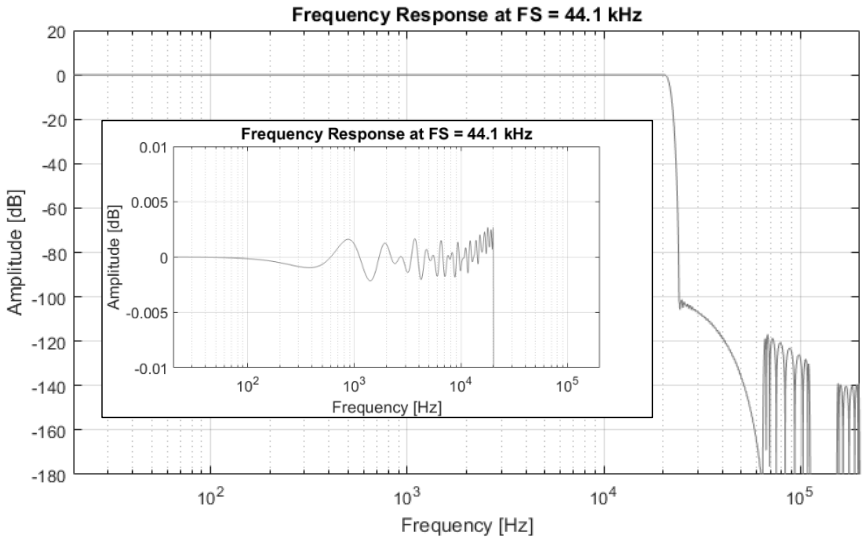
Table 23 - PCM Filter Properties

ADC: PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Frequency Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

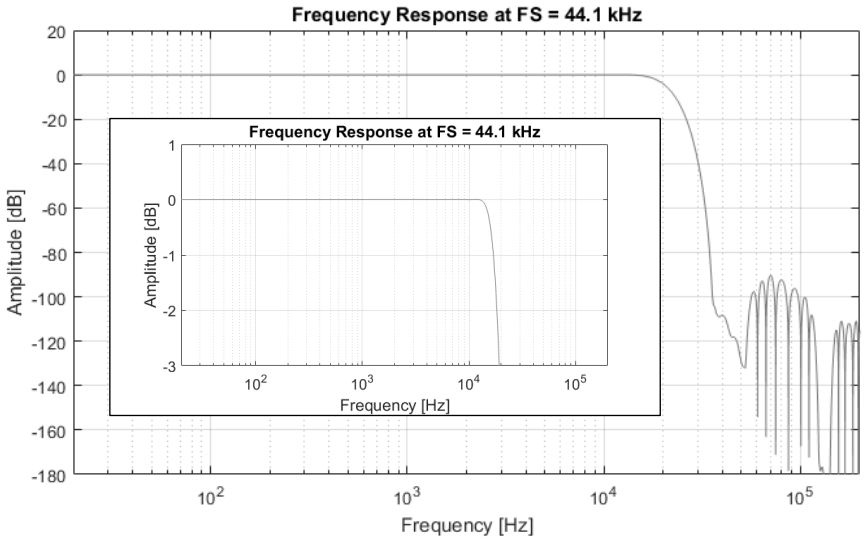
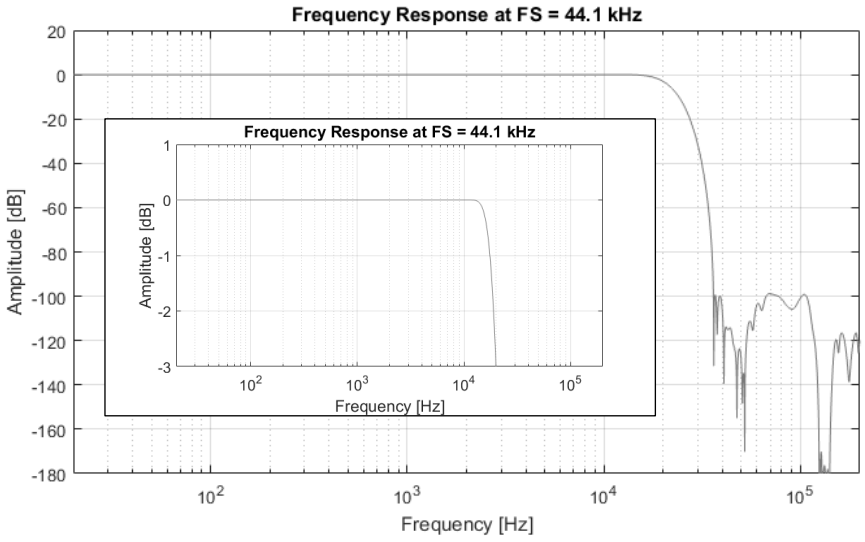
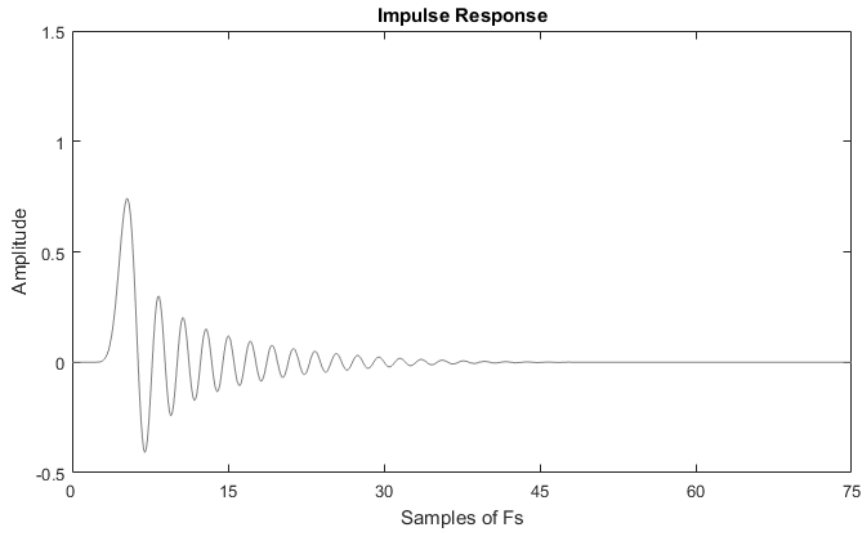
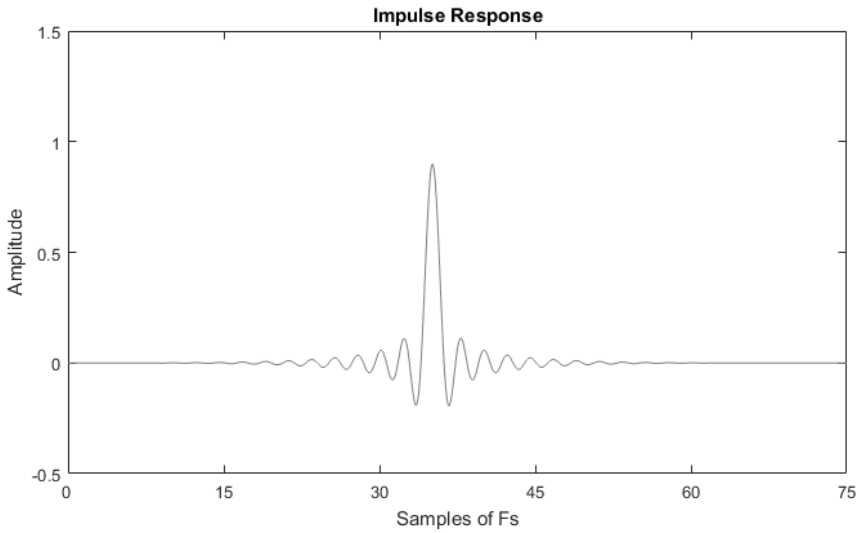
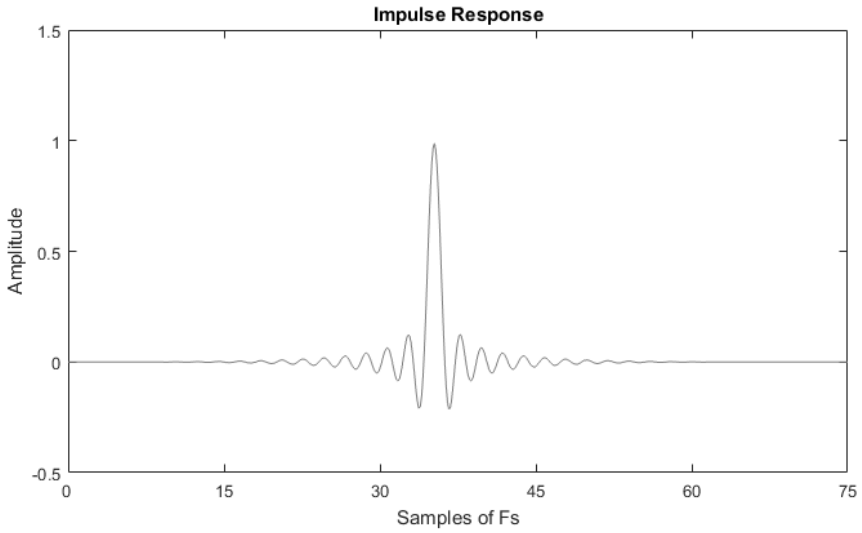
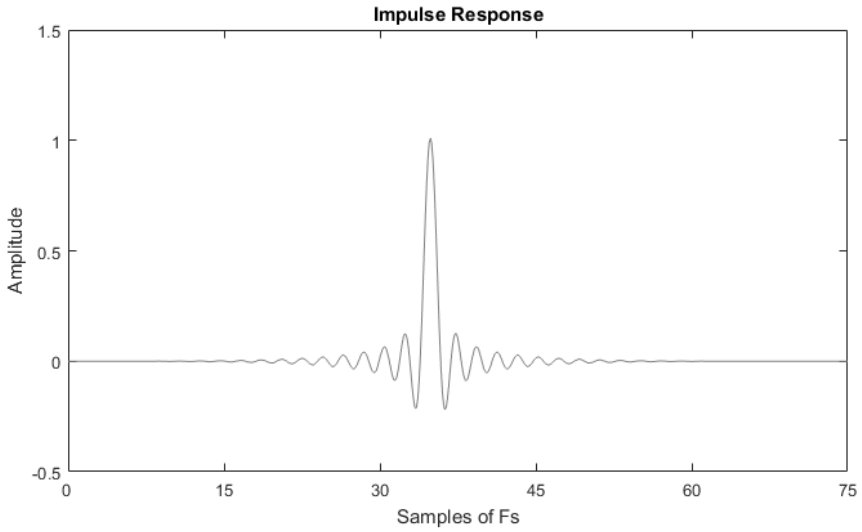
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

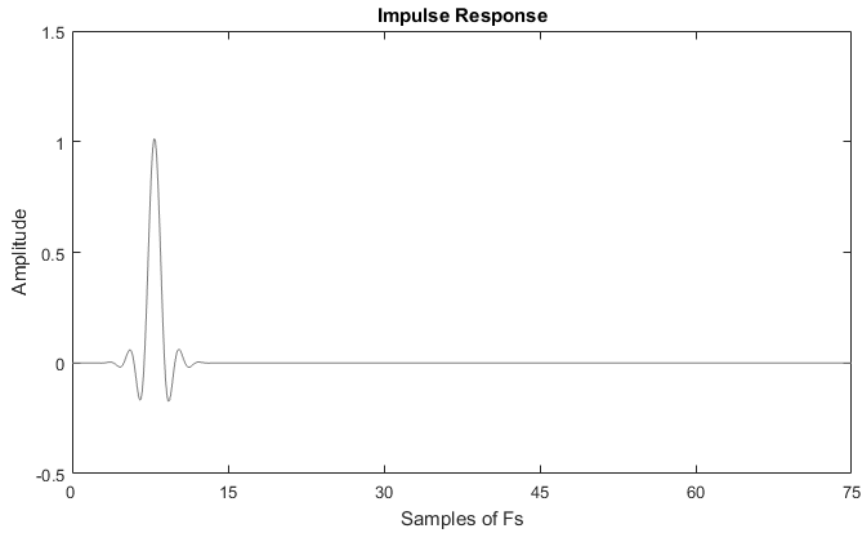
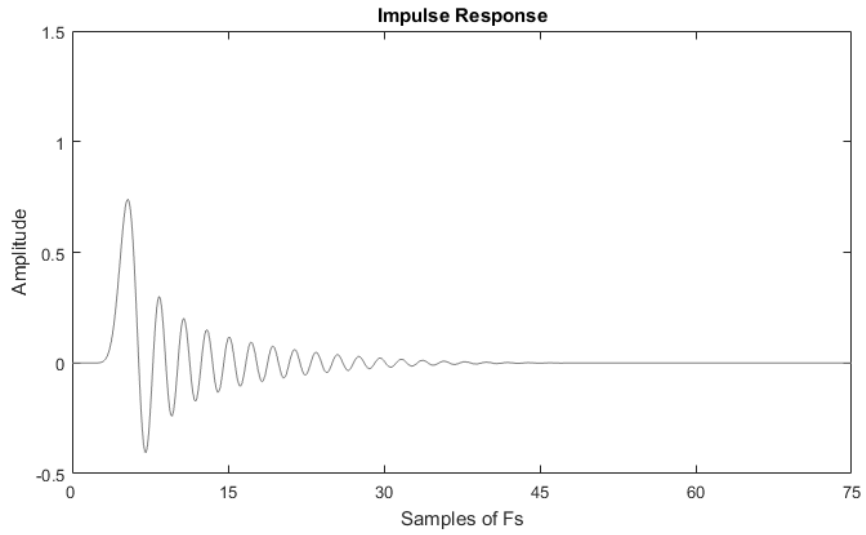
Table 24 - ADC PCM Filter Frequency Response

ADC: PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. They show the decimation path prior to down-sampling to 1FS and are scaled accordingly. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

Filter	Impulse Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

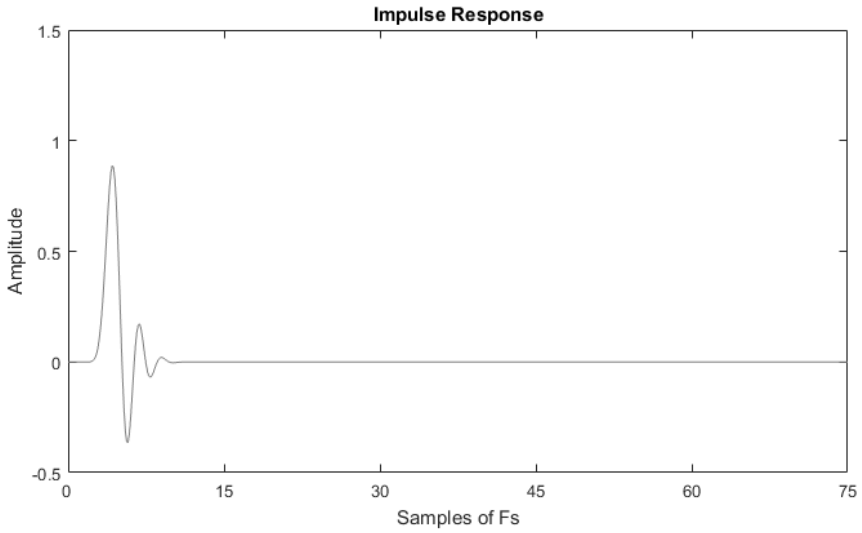
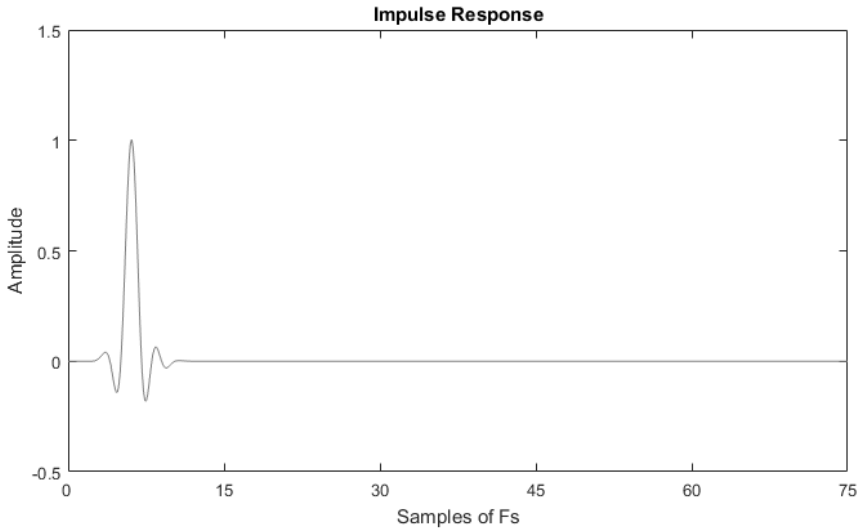
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

Table 25 - ADC PCM Filter Impulse Response

ADC: 64FS Mode

When 64FS (MCLK/FS ratio) is required, it is necessary for the ES9292PRO to be running in 64FS Mode. 64FS Mode can be manually entered by setting ENABLE_64FS_MODE to 1'b1, overriding the AUTO_FS_DETECT logic.

If using automatic sample rate detection with AUTO_FS_DETECT, 64FS Mode can be automatically accessed, unless AUTO_FS_DETECT_BLOCK_64FS is set to 1'b1.

Software Registers

- Register 1[2] ENABLE_64FS_MODE
  - Use for 64FS ratios, including 705.6/768kHz
- Register 1[0] AUTO_FS_DETECT
  - 1'b0: Manually set sample rate with Register 5 FRONT-END CLOCK CONTROL
  - 1'b1: Automatically determine the sampling rate (default)
- Register 1[1] AUTO_FS_DETECT_BLOCK_64FS
  - 1'b0: Allows AUTO_FS_DETECT to enter 64FS Mode (default)
  - 1'b1: Block AUTO_FS_DETECT from entering 64FS Mode

This mode enables the Minimum Phase 64FS filter. See filter properties.

ADC: Minimum Phase 64FS Mode Latency

The following table shows the simulated latency at 705.6kHz sampling rate and is very similar at 768kHz. Measurements were taken from the external impulse response prior to being down sampled to 1FS. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

Digital Filter	Delay
Minimum Phase Double Rate	5.5 / FS

Table 26 - ADC Minimum Phase 64FS Latency

ADC: Minimum Phase 64FS Mode Properties

Minimum Phase 64FS Mode					
Parameter	Conditions	MIN	TYP	MAX	UNIT
Pass band	-3 dB			0.44 FS	Hz
Stop band	-68.35 dB	0.68 FS			Hz
Group Delay		1.43/FS		3.45/FS	s
Flatness (ripple)					dB

Table 27 - ADC Minimum Phase 64FS Properties

ADC: Minimum Phase 64FS Mode Frequency Response

This filter gets selected automatically when MCLK/FS = 64. The following frequency response was obtained from software simulations with a sample rate of 705.6kHz

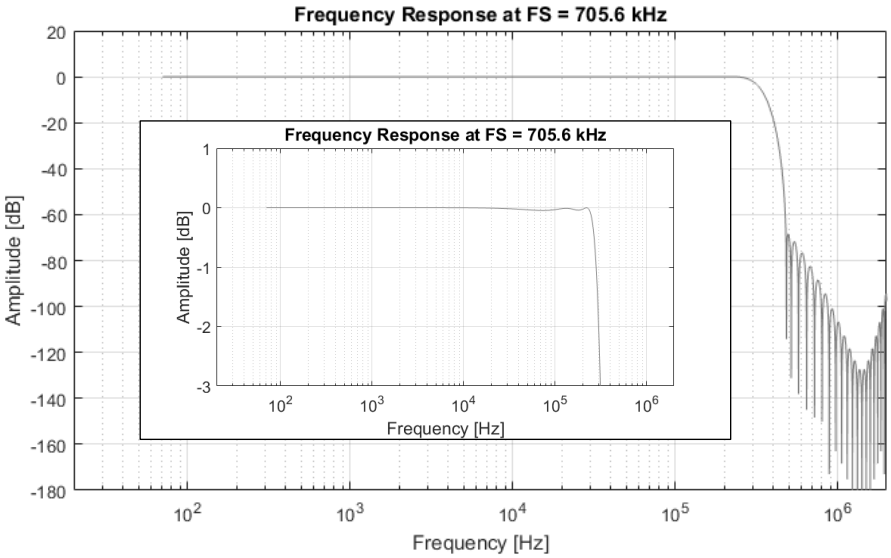


Figure 21 - ADC Minimum Phase 64FS Frequency Response

ADC: Minimum Phase 64FS Mode Impulse Response

The following impulse responses were obtained from software simulations of these filters. They show the decimation path prior to down-sampling to 1FS and are scaled accordingly. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

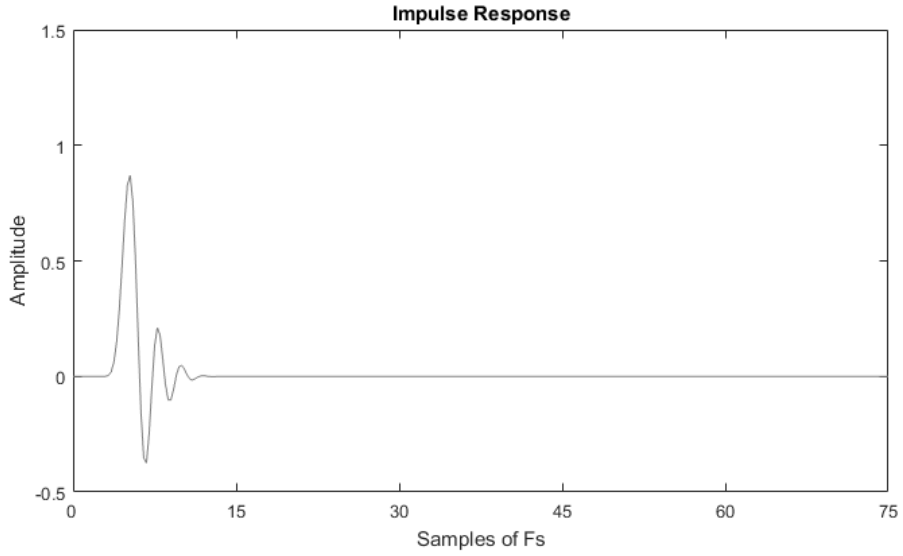


Figure 22 - ADC Minimum Phase 64FS Impulse Response

DAC: PCM Filter Latency

The following table shows the simulated latency of each filter across different sampling rates. Measurements were taken from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency will reduce (scale) with sampling rate.

Filter Shape \ Frequency [kHz]	44.1 / 48	88.2 / 96	176.4 / 192	352.8 / 384
Minimum Phase (default)	5.27 / FS	5.28 / FS	5.30 / FS	5.30 / FS
Linear Phase Apodizing Fast Roll-Off	34.64 / FS	34.65 / FS	34.65 / FS	34.66 / FS
Linear Phase Fast Roll-Off	35.28 / FS	35.28 / FS	35.28 / FS	35.29 / FS
Linear Phase Fast Roll-Off Low-Ripple	33.22 / FS	33.22 / FS	33.22 / FS	33.23 / FS
Linear Phase Slow Roll-Off	7.72 / FS	7.72 / FS	7.72 / FS	7.73 / FS
Minimum Phase Fast Roll-Off	5.29 / FS	5.29 / FS	5.29 / FS	5.30 / FS
Minimum Phase Slow Roll-Off	4.32 / FS	4.32 / FS	4.32 / FS	4.33 / FS
Minimum Phase Slow Roll-Off Low Dispersion	6.18 / FS	6.18 / FS	6.18 / FS	6.19 / FS

Table 28 - DAC PCM Filter Latency

DAC: PCM Filter Properties

Minimum Phase					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 x fs	Hz
Stop band	-95.74 dB	0.55 x fs			Hz
Group Delay		2.91/fs		9.01/fs	s
Flatness (ripple)	0.0012				dB

Linear Phase Apodizing					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.41 x fs	Hz
Stop band	-103.09 dB	0.50 x fs			Hz
Group Delay			32.81/fs		s
Flatness (ripple)	0.0028				dB

Linear Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.45 x fs	Hz
Stop band	-107.7 dB	0.55 x fs			Hz
Group Delay			33.43/fs		s
Flatness (ripple)	0.0032				dB

Linear Phase Fast Roll-Off Low Ripple					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 x fs	Hz
Stop band	-88.94 dB	0.55 x fs			Hz
Group Delay			31.37/fs		s
Flatness (ripple)	0.0013				dB

Linear Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.44 x fs	Hz
Stop band	-90.54 dB	0.75 x fs			Hz
Group Delay			5.87/fs		s
Flatness (ripple)					dB

Minimum Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 x fs	Hz
Stop band	-98.23 dB	0.55 x fs			Hz
Group Delay		2.91/fs		9.14/fs	s
Flatness (ripple)	0.0023				dB

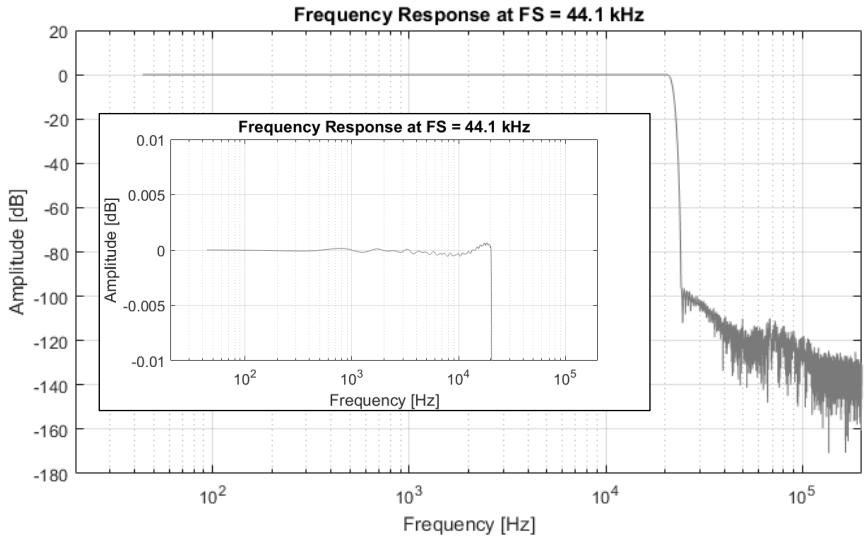
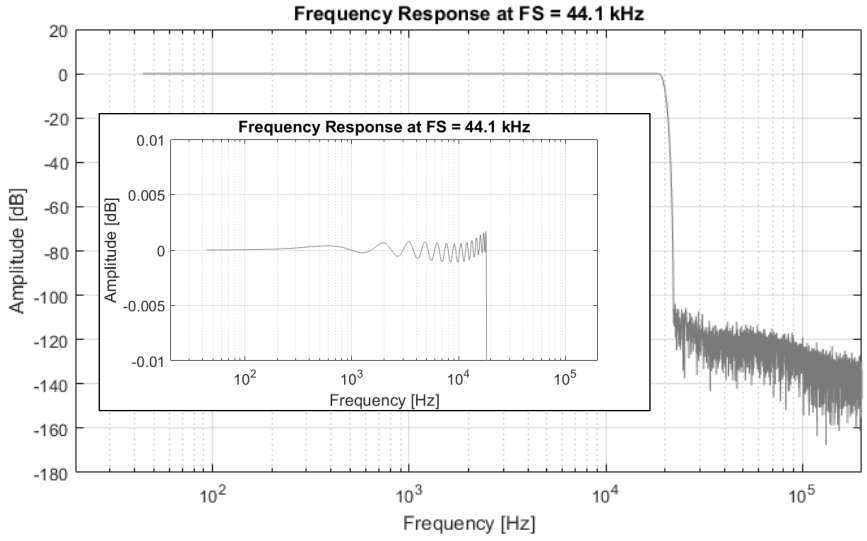
Minimum Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.43 x fs	Hz
Stop band	-90.67 dB	0.80 x fs			Hz
Group Delay		2.08/fs		3.56/fs	s
Flatness (ripple)					dB

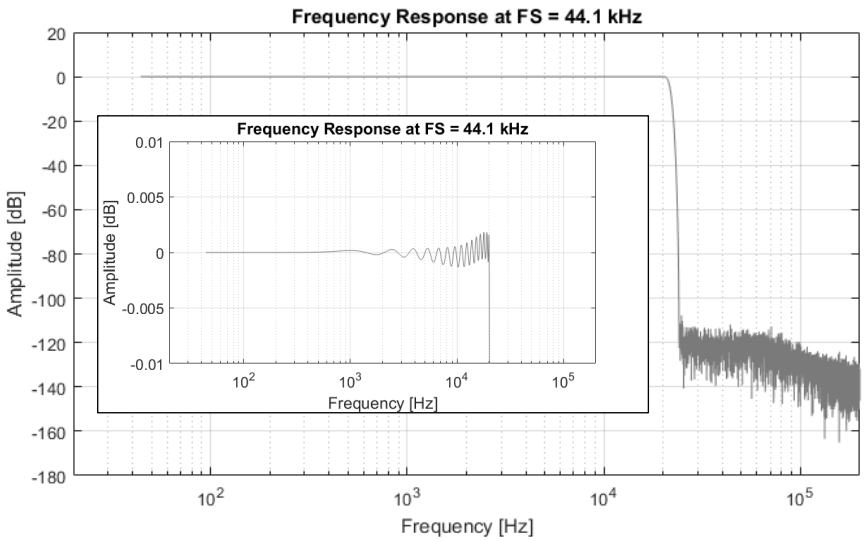
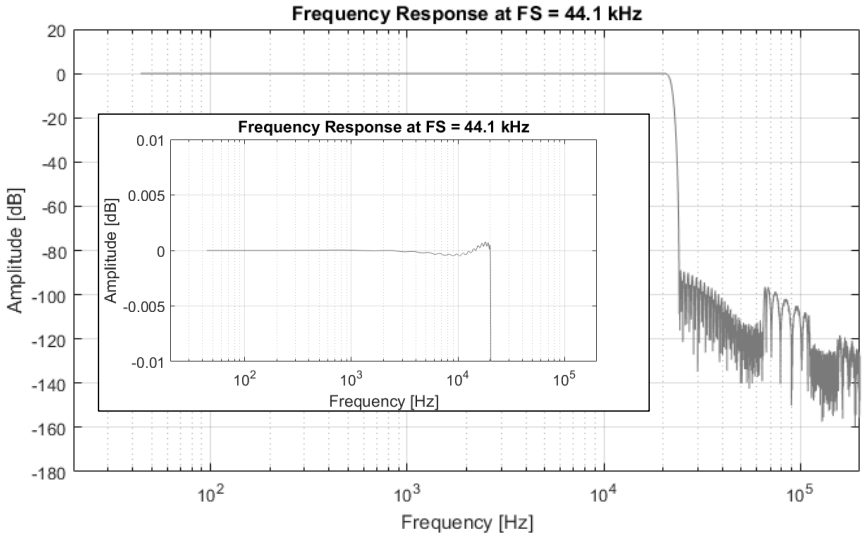
Minimum Phase Slow Roll-Off Low Dispersion					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.45 x fs	Hz
Stop band	-97.48 dB	0.82 x fs			Hz
Group Delay		4.21/fs		4.42/fs	s
Flatness (ripple)					dB

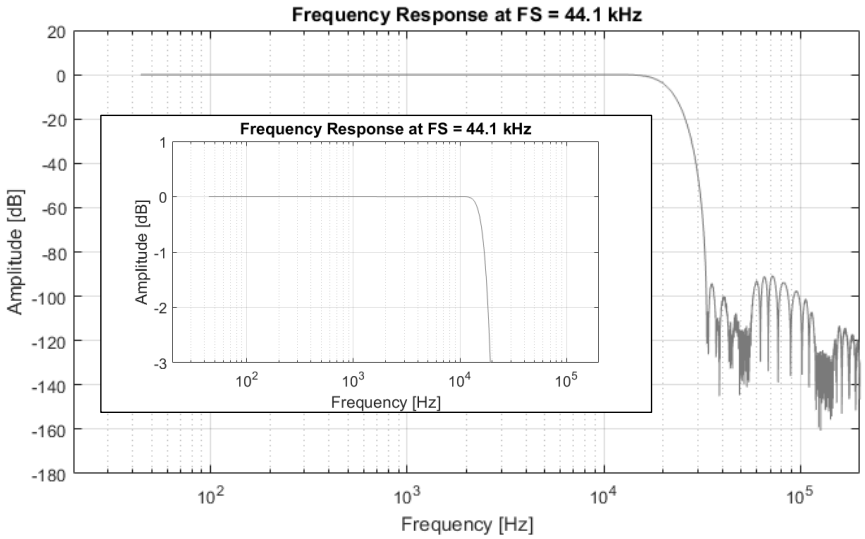
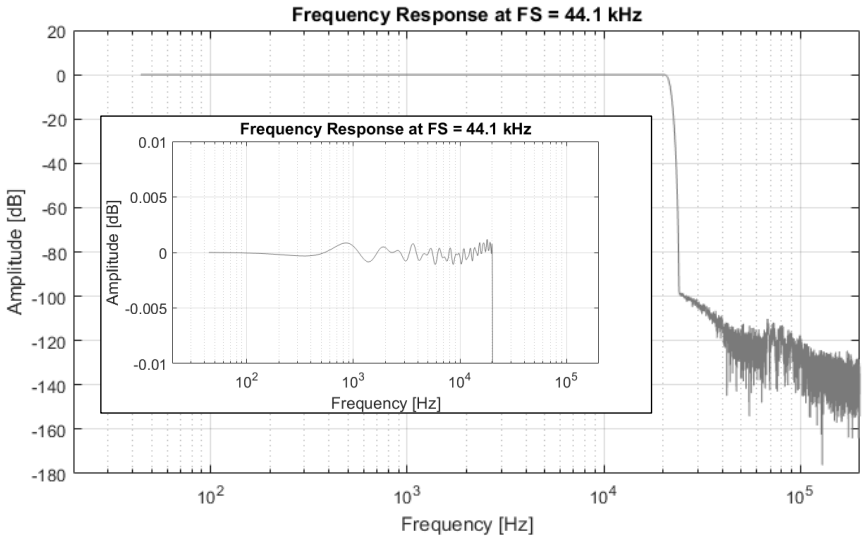
Table 29 - DAC PCM Filter Properties

DAC: PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Frequency Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

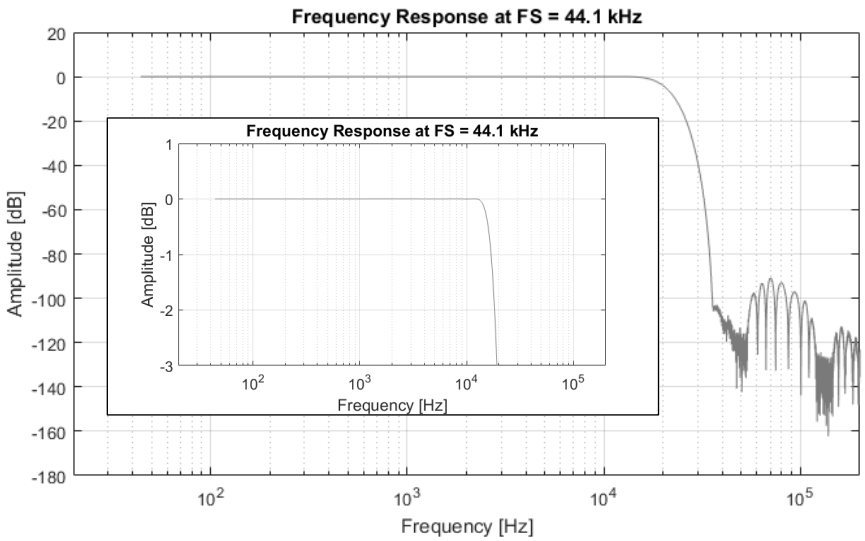
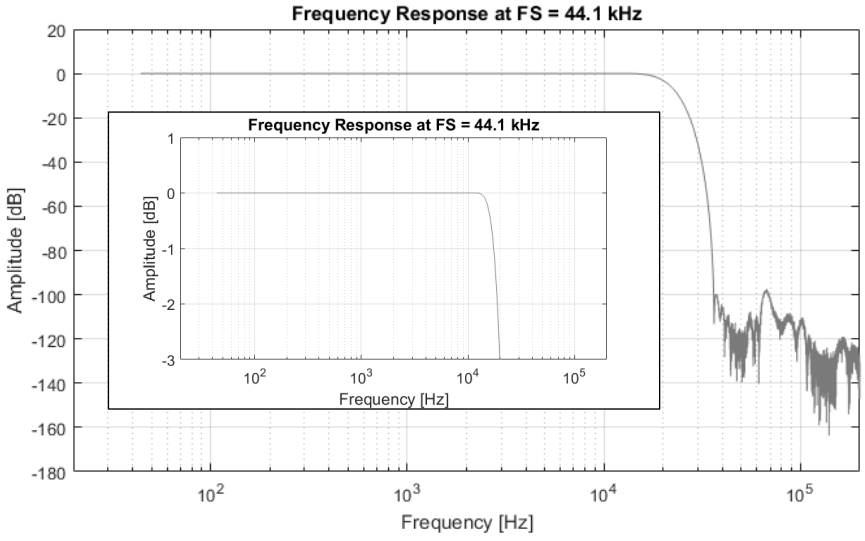
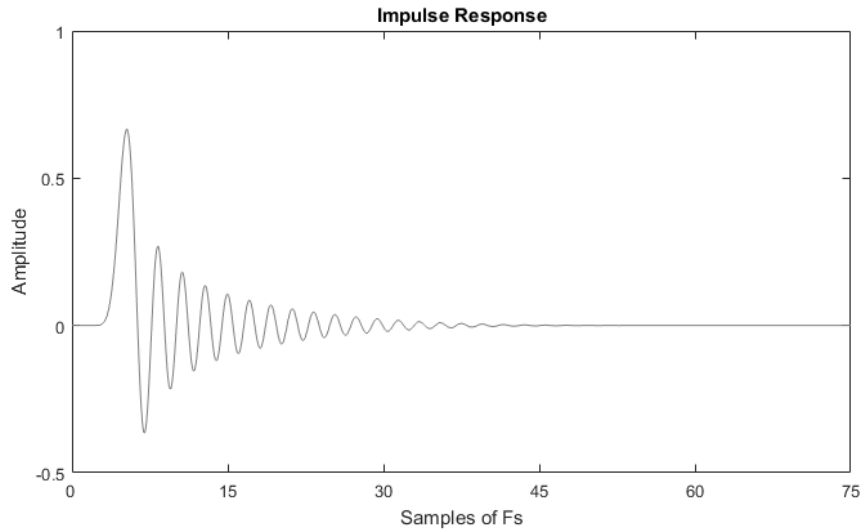
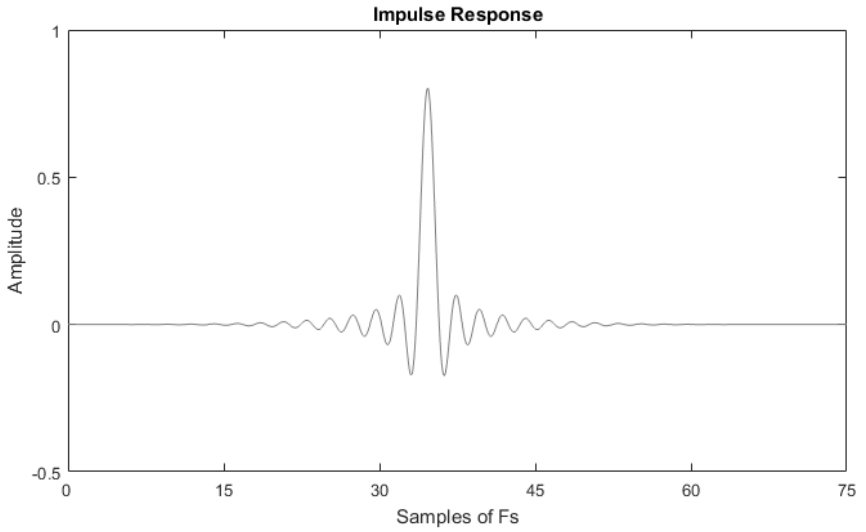
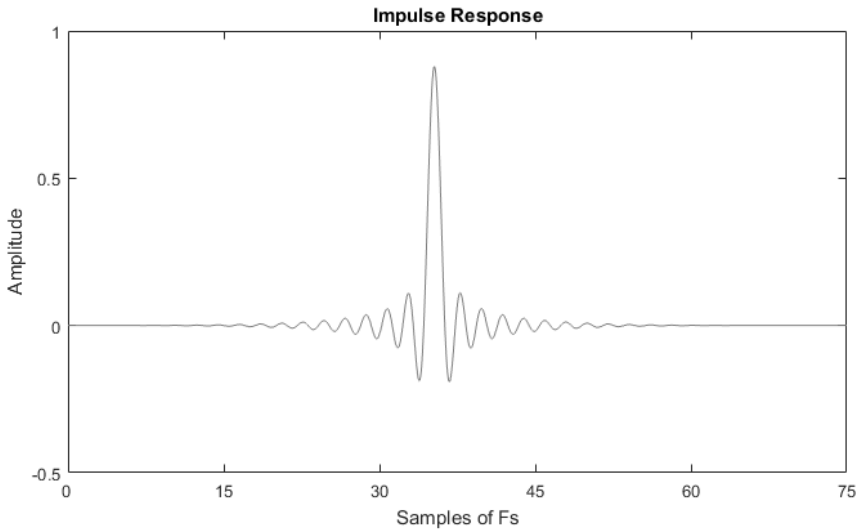
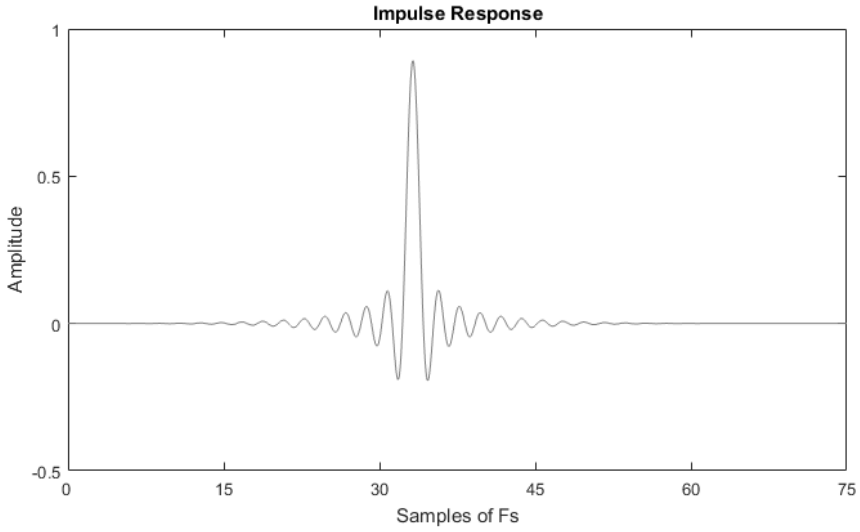
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

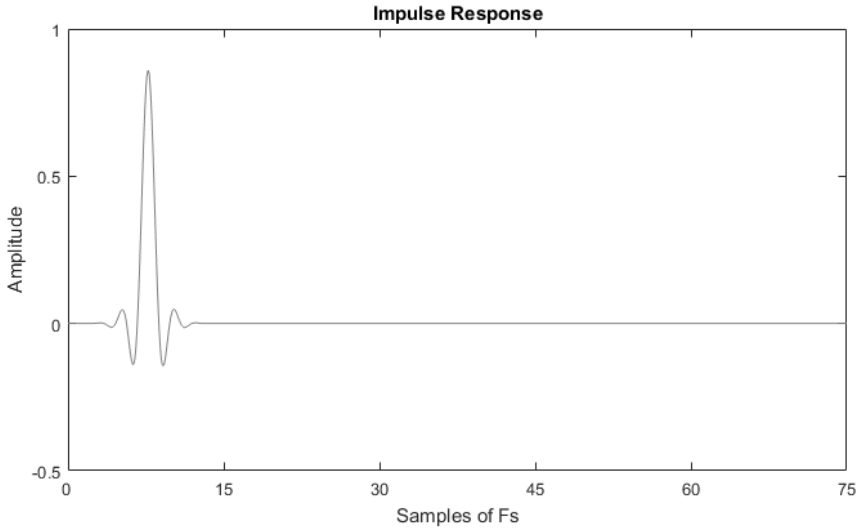
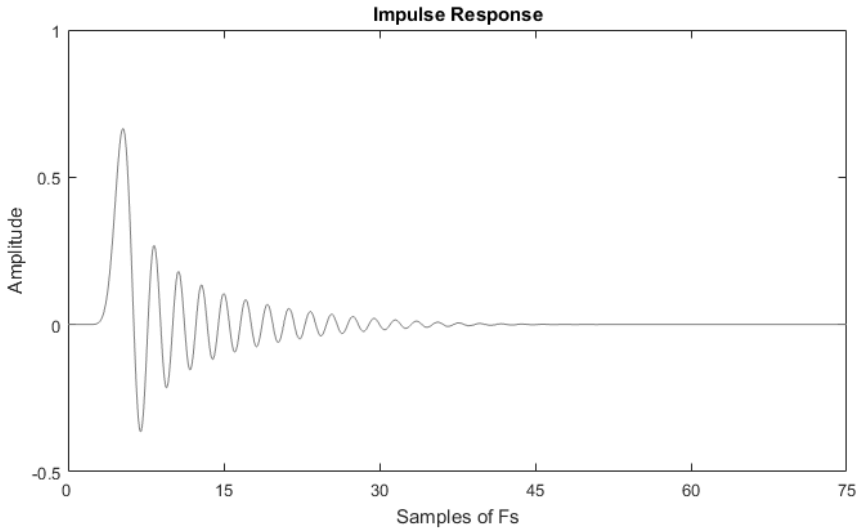
Table 30 - DAC PCM Filter Frequency Response

DAC: PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. They were measured from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

Filter	Impulse Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

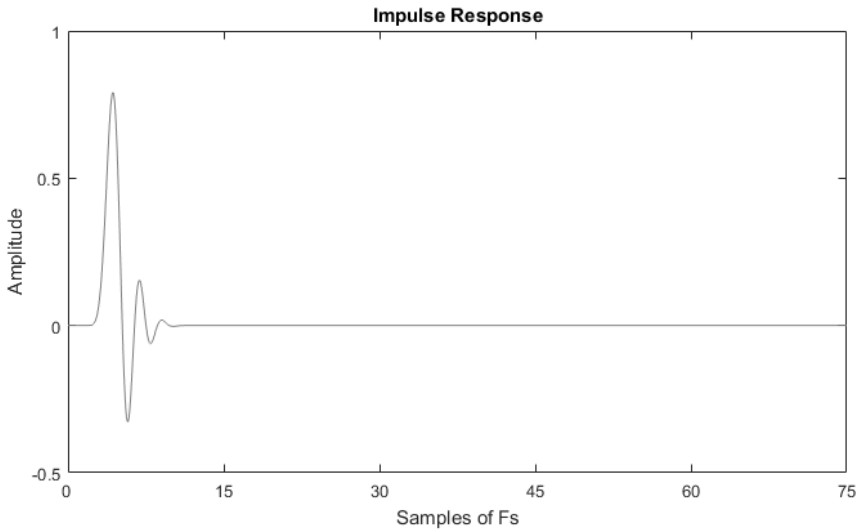
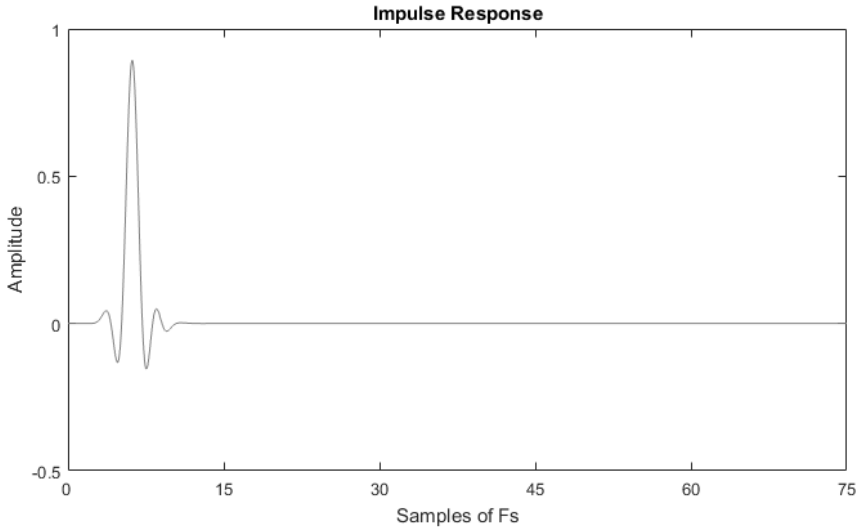
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

Table 31 - DAC PCM Filter Impulse Response

DAC: 64FS Mode

When 64FS (MCLK/FS ratio) is required, it is necessary for the ES9292PRO to be running in 64FS Mode. 64FS Mode can be manually entered by setting ENABLE_64FS_MODE to 1'b1, overriding the AUTO_FS_DETECT logic.

If using automatic sample rate detection with AUTO_FS_DETECT, 64FS Mode can be automatically accessed, unless AUTO_FS_DETECT_BLOCK_64FS is set to 1'b1.

Software Registers

- Register 1[2] ENABLE_64FS_MODE
  - Use for 64FS ratios, including 705.6/768kHz
- Register 1[0] AUTO_FS_DETECT
  - 1'b0: Manually set sample rate with Register 5 FRONT-END CLOCK CONTROL
  - 1'b1: Automatically determine the sampling rate (default)
- Register 1[1] AUTO_FS_DETECT_BLOCK_64FS
  - 1'b0: Allows AUTO_FS_DETECT to enter 64FS Mode (default)
  - 1'b1: Block AUTO_FS_DETECT from entering 64FS Mode

This mode enables the Minimum Phase 64FS filter. See filter properties.

DAC: Minimum Phase 64FS Mode Latency

The following table shows the simulated latency at 705.6kHz sampling rate and is very similar at 768kHz. Measurements were taken from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

Digital Filter	Delay(us) @ FS = 705.6 kHz
Minimum Phase Double Rate	3.61 / FS

Table 32 - DAC Minimum Phase 64FS Latency

DAC: Minimum Phase 64FS Mode Properties

Minimum Phase 64FS Mode					
Parameter	Conditions	MIN	TYP	MAX	UNIT
Pass band	-3 dB			0.45 x fs	Hz
Stop band	-61.3 dB	0.68 x fs			Hz
Group Delay		1.54/fs		2.35/fs	s
Flatness (ripple)					dB

Table 33 - DAC Minimum Phase 64FS Properties

DAC: Minimum Phase 64FS Mode Frequency Response

This filter gets selected automatically when MCLK/FS = 64. The following frequency response was obtained from software simulations with a sample rate of 705.6kHz

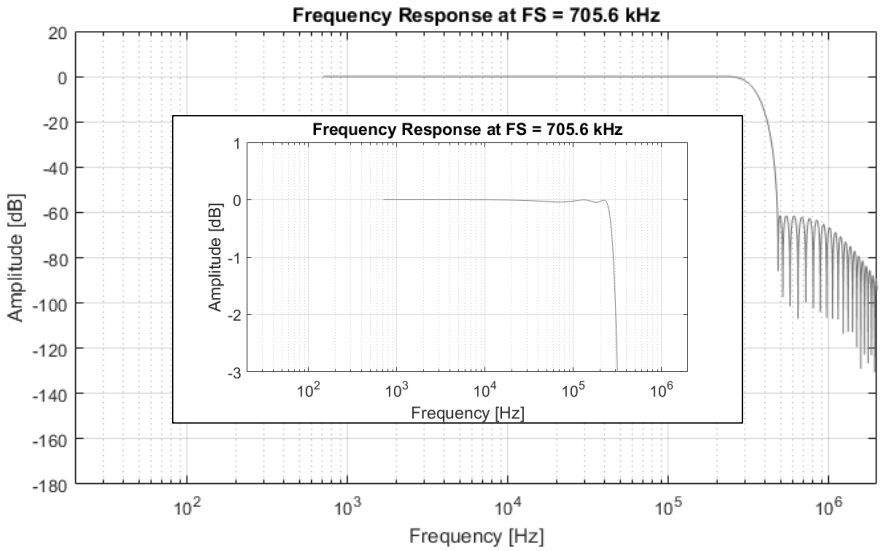


Figure 23 - DAC Minimum Phase 64FS Frequency Response

DAC: Minimum Phase 64FS Mode Impulse Response

The following impulse responses were obtained from software simulations of these filters. They were measured from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

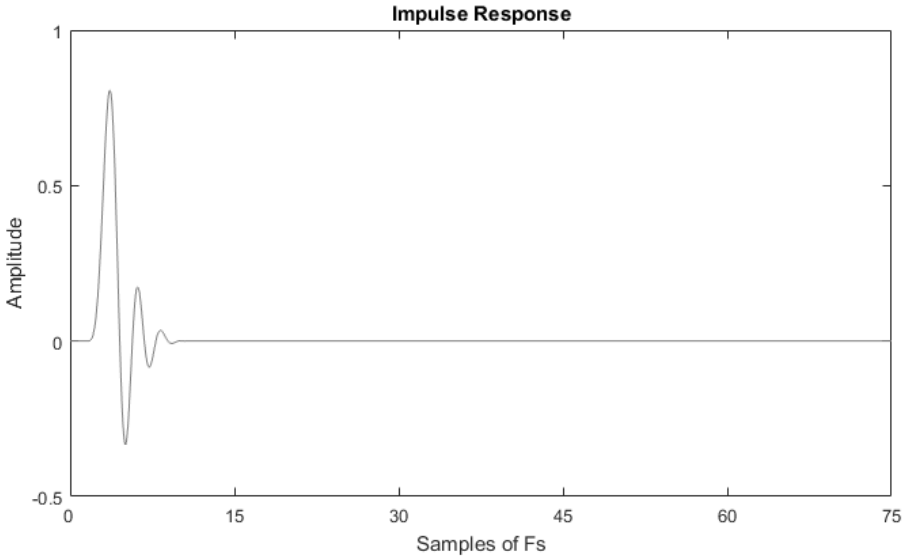


Figure 24 - DAC Minimum Phase 64FS Impulse Response

Sample Rate Calculation

Acquiring the real time sample rate from the ES9292PRO can be accomplished using Register 220 AUTO FS READ.

Auto fs detect (Register 1[0] AUTO_FS_DETECT = 1'b1) must be set.

The below equation calculates the current auto detected sample rate by using a combination of register readback states.

$$FS\ [Hz] = \frac{Y * MCLK}{(X+1) * \left(\frac{128}{2^Z}\right)}$$

Variables

- {X}: Register 232[5:0] MCLK_128FS_DIV_AUTO
- {Y}: Register 232[6] MCLK_128FS_HALF_DIV_AUTO
  - 1'b0: Y=1
  - 1'b1: Y=2
- {Z}: Register 232[7] EN_64FS_MODE_AUTO
- MCLK: Master Clock rate

Example

For this example, let the variables be as follows:
X = 7, Y = 1, Z = 0, MCLK = 49.152 [MHz]

$$FS\ [Hz] = \frac{1 * 49.152MHz}{(7+1) * \left(\frac{128}{2^0}\right)} = \frac{49.152MHz}{8 * 128} = 48kHz$$

TDM Daisy Chain Mode

The ES9292PRO supports connections multiple devices together in daisy chain configuration. Up to 16 devices can be daisy chained together to output data onto any of the 32 channels in a TDM data line. The DAC's Daisy Chain has a digital input on DATA4 from the previous chip and will take the respective channel's data for conversion and pass the TDM data to be output on GPIO2 for the next chip down the chain. At the same time, the ADC's Daisy Chain has a digital input on GPIO1 from the previous chip and will append that device's data onto the line and output on DATA2. See Application Note for more information.

To set up TDM Daisy Chain mode, enable TDM_xxx_DAISY_CHAIN and select the total channel count with TDM_CH_NUM, then set the TDM_xxx_DATA_LATCH_ADJ registers based on the chip's location in the chain. The central number in each chip in Figure 25 denotes the TDM_xxx_DATA_LATCH_ADJ value for that device.

Note: GPIO1 on the last ES9292PRO of the Daisy Chain must be set to zero by tying to ground through a 47Ω resistor.

Data Path	Output Pin	Input Pin
DAC	GPIO2/DATA5	DATA4
ADC	DATA2	GPIO1/DATA3

Table 34 - Daisy Chain Pins

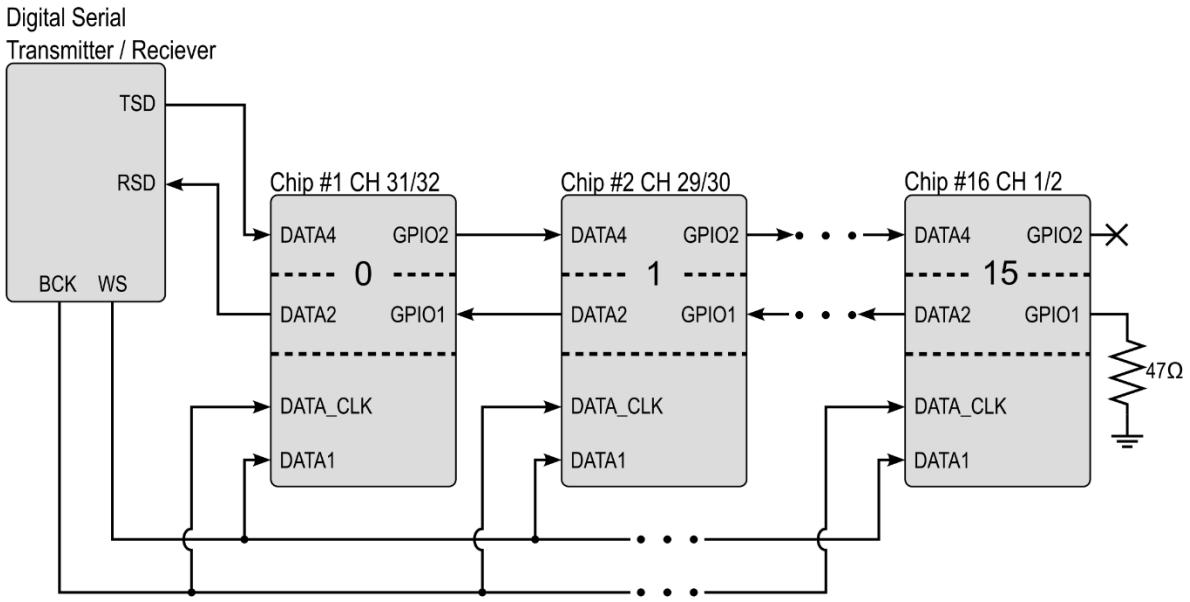


Figure 25 - TDM Daisy Chain Configuration

TDM Daisy Chain Registers

- Register 10[4:0] TDM_CH_NUM
- Register 16[7] TDM_ENC_DAISY_CHAIN
- Register 16[4:0] TDM_ENC_DATA_LATCH_ADJ
- Register 17[7] TDM_DEC_DAISY_CHAIN
- Register 17[4:0] TDM_DEC_DATA_LATCH_ADJ

TDM Parallel Mode

The ES9292PRO also supports TDM in parallel mode. In this case, the chips will simply connect the output or input data lines together. Each chip will input or output data during the designed slots during a single gram of the TDM data line, then switch to high impedance so that the next chip may input or output its data onto the data lines. To set up TDM Parallel mode, select the total channel count with TDM_CH_NUM, and set the desired slots with the PCM/TDM Encoder/Decoder Mapping Registers.

Note: TDM Parallel Mode supports left-justified and I²S (TDM_CH_NUM ≥ 1)

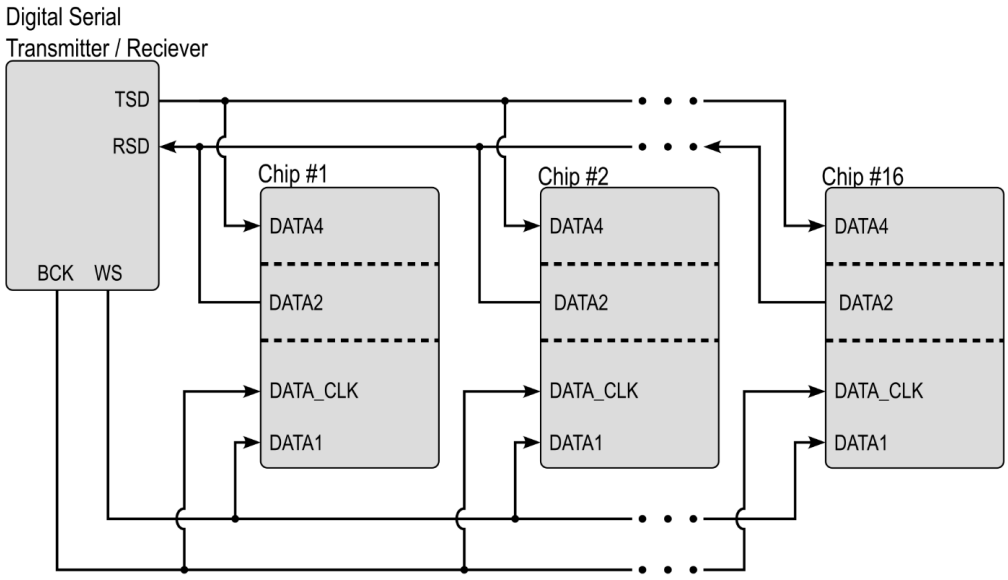


Figure 26 - TDM Parallel Configuration

TDM Parallel Registers

- Register 10[4:0] TDM_CH_NUM

PCM/TDM Encoder Mapping Registers

- Register 12-13[4:0] TDM_ENC_SLOT_SEL_CH1
- Register 12-13[12:8] TDM_ENC_SLOT_SEL_CH2

PCM/TDM Decoder Mapping Registers

- Register 14-15[4:0] TDM_DEC_SLOT_SEL_CH1
- Register 14-15[12:8] TDM_DEC_SLOT_SEL_CH2

THD Compensation

The ES9292PRO has integrated ADC and DAC THD Compensation to add or correct second and third harmonics that may be present on the output signal. The compensation is controlled by two signed 16-bit coefficients for the ADC Datapath located in Registers 93-96 and two signed 12-bit coefficients for the DAC Datapath located in Registers 127-130.

The following equation displays how the second and third order harmonics are affected by the C2 and C3 values:

$$output = x + c2 * x^2 + c3 * x^3$$

ADC THD Compensation Coefficient Registers

- Registers 93-94: ADC THD COMP C2
- Registers 95-96: ADC THD COMP C3

DAC THD Compensation Coefficient Registers

- Registers 127-128: DAC THD COMP C2
- Registers 129-130: DAC THD COMP C3

Zero Cross Detection

The ES9292PROs ADC and DAC paths integrate a Zero Cross Detection block to flag when the signal has a zero cross. The result can be output on a GPIO, see GPIO Configuration for more information. The live or latched result can be read from the readback Register 233 and 242.

Zero Cross Detection Registers

- Register 42[7, 6] MASK_DAC_XCD_CHx
- Register 43[7, 6] CLEAR_DAC_ZCD_CHx
- Register 76[3:2, 1:0] ADC_CHx_DET_FLAG_SEL = 2'd2 (ADC Zero-Cross Detect Flag)
- Register 97[5, 4] ADC_ZCD_EN_CHx
- Register 115[7, 6] DAC_ZCD_EN_CHx
- Register 233 [3, 2] ADC_ZERO_CROSS_LAT_CHx
- Register 233 [1, 0] ADC_ZERO_CROSS_CHx
- Register 242 [3, 2] DAC_ZERO_CROSS_LAT_CHx
- Register 242 [1, 0] DAC_ZERO_CROSS_CHx

SPI Master Zero Cross Detect

The Zero Cross Detection Operation allows the SPI Master to send commands to an external peripheral when the input signal has a zero cross. This operation is very useful when interacting with PGAs (Programmable Gain Amplifiers) as they require a gain change at a zero cross to minimize noise and transient signals. Zero Cross Detect Operation is only available for SSM2 and SSM3.

For more information on the Zero Cross Detect Operation of the SPI Master Interface please ask your FAE or Distributor for the SPI Master Application Note.

ASP2 DMA Zero Cross Detect

The Zero Cross Detection Operation allows the ASP2s DMA to update coefficients when the input signal has a zero cross. This operation is very useful when updating coefficients related to gain changes or processing paths to minimize noise and transient signals.

For more information on the Zero Cross Detect Operation of the ASP2 please ask your FAE or Distributor for the SPI Master Application Note.

Clock Distribution

The ES9292PRO includes features for selecting and manipulating the input clock sources to various blocks of the device.

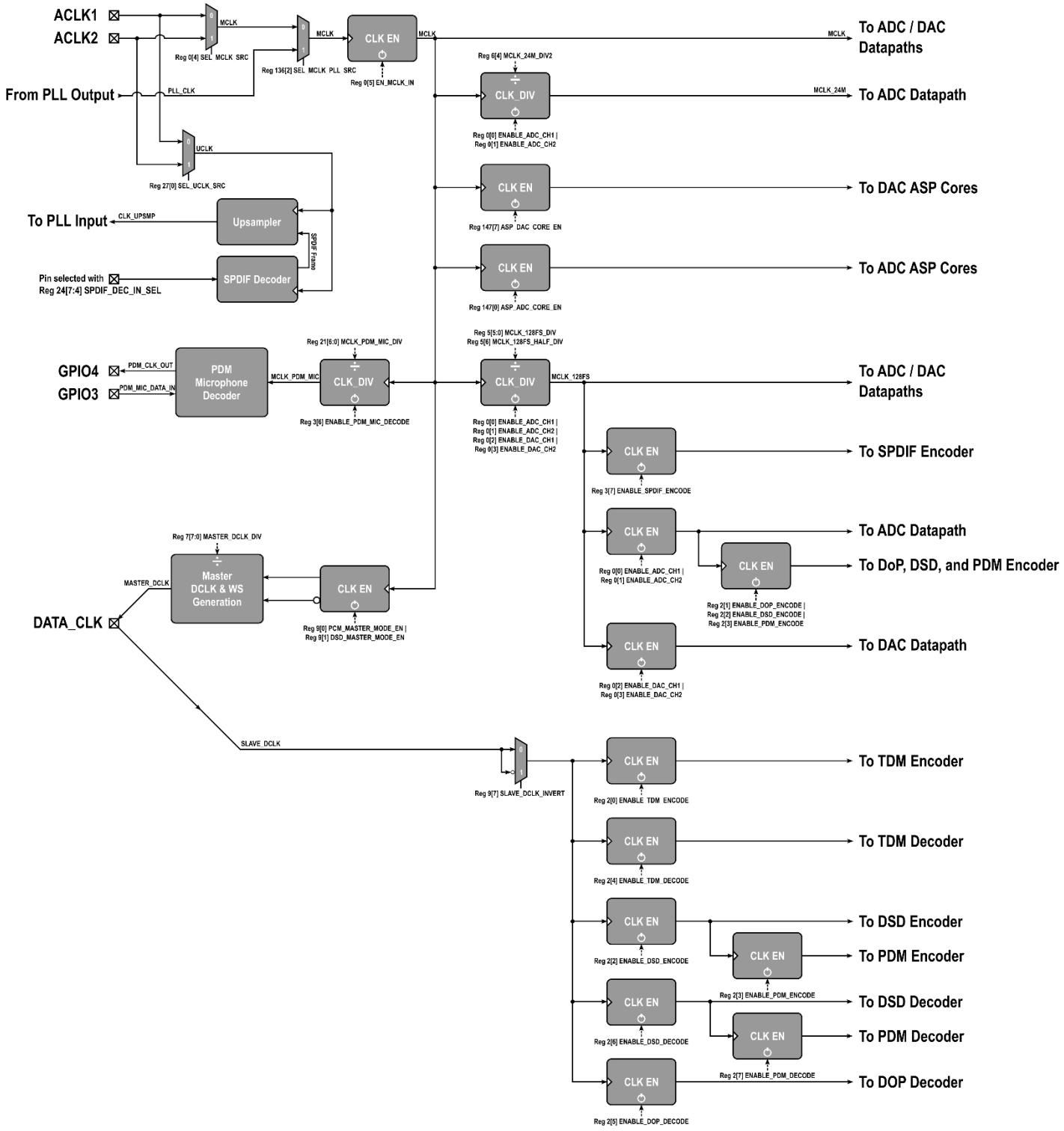


Figure 27 - Clock Distribution

The following list shows the various clocks of the ES9292PRO and the associated registers for configuration.

MCLK

The MCLK source to the device can be enabled and selected between ACLK1, ACLK2, or PLL_CLK with the following registers.

- Register 0[5] EN_MCLK_IN
- Register 0[4] SEL_MCLK_SRC
- Register 136[2] SEL_MCLK_PLL_SRC

MCLK_24M

MCLK_24M is required by the ADC Datapath to be 22.5792 / 24.576MHz respectively The DIV2 bit must be set when using an MCLK of 45.1584 / 49.152MHz.

- Register 6[4] MCLK_24M_DIV2
- Register 0[0,1] ENABLE_ADC_CHx

MCLK_128FS

MCLK_128FS must be tuned such that $\mathrm{MCLK} * \frac{2^{\mathrm{MCLK\_128FS\_HALF\_DIV}}}{\mathrm{MCLK\_128FS\_DIV}} = \mathrm{MCLK\_128FS} = 128 * \mathrm{FS}$. This ratio is automatically tuned by default with AUTO_FS_DETECT. A ratio of 64 for higher sample rates can be achieved with ENABLE_64FS_MODE.

- Register 5[6] MCLK_128FS_HALF_DIV
- Register 5[5:0] MCLK_128FS_DIV
- Register 1[0] AUTO_FS_DETECT
- Register 1[1] AUTO_FS_DETECT_BLOCK_64FS
- Register 1[2] ENABLE_64FS_MODE

Master DCLK

The Master DCLK & WS Generation block is enabled when either PCM or DSD Master Mode is enabled. The generated DCLK is output on the DATA_CLK pin, and the frequency is set with the divider register.

- Register 9[0] PCM_MASTER_MODE_EN
- Register 9[1] DSD_MASTER_MODE_EN
- Register 7[7:0] MASTER_DCLK_DIV
- Register 9[5] MASTER_WS_CLK_PHASE
- Register 9[4] MASTER_WS_PULSE_MODE
- Register 9[3] MASTER_WS_INVERT
- Register 9[2] MASTER_DCLK_INVERT

Slave DCLK

The input Slave DCLK is sourced from the DATA_CLK pin, which means a DCLK provided externally or generated internally.

- Register 9[7] SLAVE_DCLK_INVERT

MCLK_PDM_MIC

The PDM Microphone Decoder clock is enabled and divided with the below registers.

- Register 3[6] ENABLE_PDM_MIC_DECODE
- Register 21[6:0] MCLK_PDM_MIC_DIV

UCLK

The ES9292PROs UCLK is used by the S/PDIF Decoder and UPSAMPLER. The source can be selected between ACLK1 and ACLK2.

- Register 27[0] SEL_UCLK_SRC

CLK_UPSMP

CLK_UPSMP is the output clock from the UPSAMPLER to be used by the APLL to generate an MCLK source for the device.

Analog Features

APLL

The ES9292PRO has a built in Analog PLL (APLL) for generating frequencies that are unavailable externally. For an application note on the APLL, please ask your FAE or Distributor for availability.

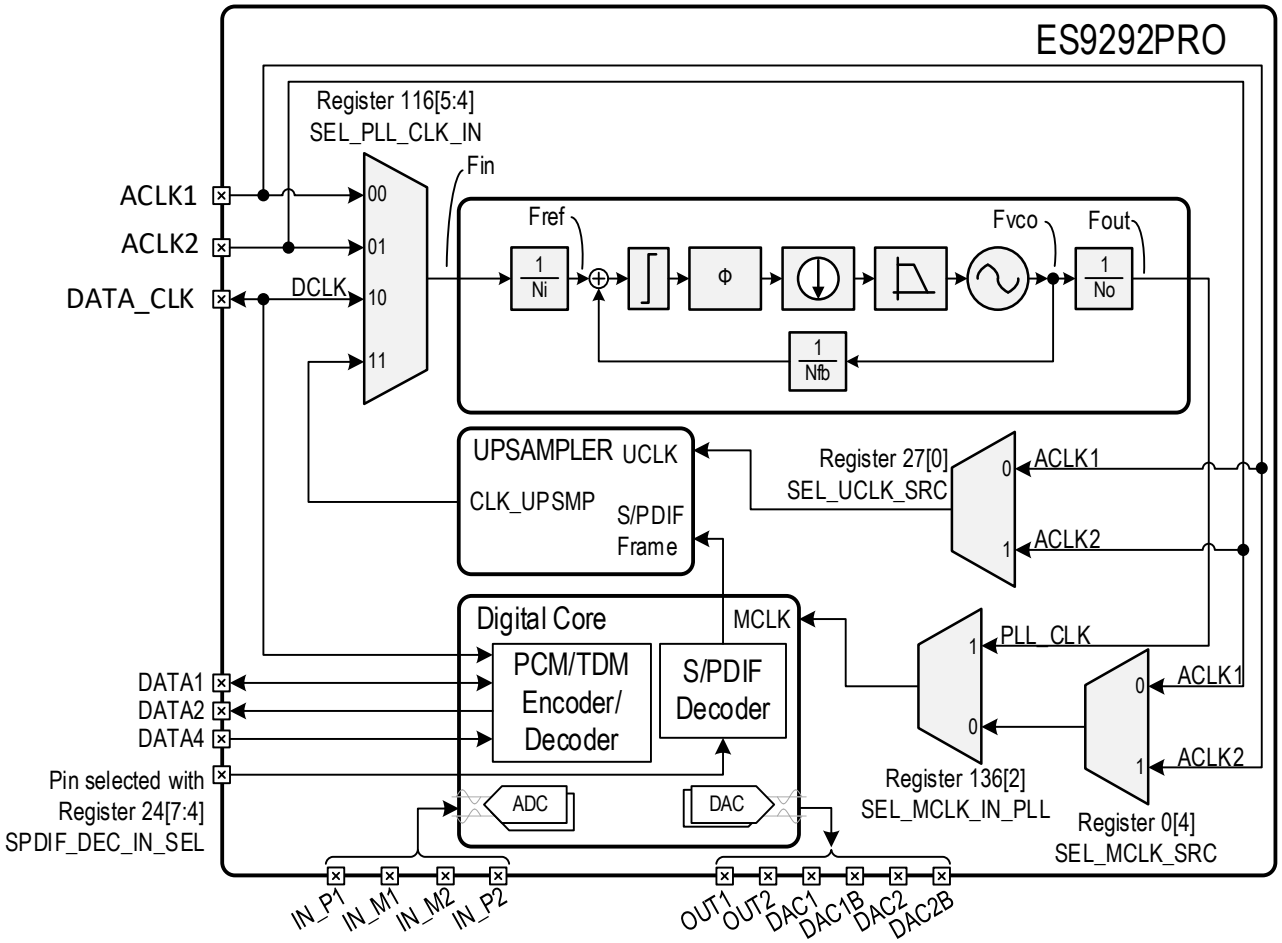


Figure 28 - Functional Block Diagram of ES9292PRO APLL with Upsampler

The input clock (F_{in}) source to the APLL is chosen between ACLK1, ACLK2, DCLK, or CLK_UPSMP with Register 116[5:4] SEL_PLL_CLK_IN. The MCLK source to the chip is chosen between the APLLs output or either of the ACLK pins with Registers 0[4] SEL_MCLK_SRC and 136[2] SEL_MCLK_IN_PLL.

Frequency Output Dividers

For calculation of the PLLs output frequency, use the following formulas:

$$F_{ref} = \left(\frac{F_{in}}{N_i}\right) \qquad F_{vco} = \left(\frac{F_{in}}{N_i}\right) * N_{fb} \qquad N_{fb} = \frac{2^{25}}{FBDIV} \qquad F_{out} = \left(\frac{F_{in}}{N_i}\right) * \frac{N_{fb}}{N_o}$$

Where:

- PLL frequency range requirements:
  - Fref: 2.5MHz < Fref < 13MHz
  - Fvco: 90MHz < Fvco < 110MHz
  - Fout: 22.5792/24.576MHz or 45.1584/49.152MHz
- Ni = Input Divider (Reg 122-124[8:0]) = (PLL_CLK_IN_DIV + 1)
- No = Output Divider (Reg 122-124[15:12]) = (PLL_CLK_OUT_DIV + 1)
- FBDIV = 24-bit number (Reg 119-121[23:0])
  - Toggle Reg 122-124[9] PLL_FB_DIV_LOAD to load PLL_CLK_FB_DIV value)
- Nfb = Feedback Divider

44.1kHz Base Rates (SYNC Slave Mode)							
FS (kHz)	**DCLK (MHz)**	**Ni**	**Fref (MHz)**	**FBDIV**	**Fvco (MHz)**	**No**	**Fout (MHz)**
32-Bit Frame							
352.8	22.5792	2	11.2896	4194304	90.3168	4	22.5792
176.4	11.2896	1	11.2896	4194304	90.3168	4	22.5792
88.2	5.6448	1	5.6448	2097152	90.3168	4	22.5792
44.1	2.8224	1	2.8224	1048576	90.3168	4	22.5792
16-Bit Frame							
352.8	11.2896	1	11.2896	4194304	90.3168	4	22.5792
176.4	5.6448	1	5.6448	2097152	90.3168	4	22.5792
88.2	2.8224	1	2.8224	1048576	90.3168	4	22.5792
44.1	1.4112	1	1.4112	524288	90.3168	4	22.5792

Table 35 - APLL Divider Values for 44.1kHz Base Rates

48kHz Base Rates (SYNC Slave Mode)							
FS (kHz)	**DLK (MHz)**	**Ni**	**Fref (MHz)**	**FBDIV**	**Fvco (MHz)**	**No**	**Fout (MHz)**
32-Bit Frame							
384	24.576	2	12.288	4194304	98.304	4	24.576
192	12.288	1	12.288	4194304	98.304	4	24.576
96	6.144	1	6.144	2097152	98.304	4	24.576
48	3.072	1	3.072	1048576	98.304	4	24.576
16-Bit Frame							
384	12.288	1	12.288	4194304	98.304	4	24.576
192	6.144	1	6.144	2097152	98.304	4	24.576
96	3.072	1	3.072	1048576	98.304	4	24.576
48	1.536	1	1.536	524288	98.304	4	24.576

Table 36 - APLL Divider Values for 48kHz Base Rates

Upsampler

The Clock Upsampler synthesizes a low-jitter output clock from a low-frequency reference. A downstream multiplying analog PLL (APLL) then removes the resulting out-of-band noise-shaping quantization noise while scaling to the desired final frequency, yielding a clean output clock whose jitter is governed by the Upsampler bandwidth at low offset frequencies and by the analog PLL bandwidth at higher offset frequencies. The clock source for the Upsampler can be ACLK S/PDIF.

The Upsampler runs on an Asynchronous ACLK, with register defaults tuned to 50MHz, but can be lowered down to 38MHz. The low-frequency reference for the Upsampler is the S/PDIF decoder frame. The Upsampler can be used to synthesize a MCLK that is synchronous to the S/PDIF frame, which can then be used by the rest of the ES9292PRO.

For more information on the Upsampler and its operation please see the S/PDIF Decoder section and ask your FAE or Distributor for the availability of the Upsampler Application Note.

MCLK Configurations

The ES9292PRO features multiple methods of supplying an MCLK to the chip. Direct ACLK1/2 pin connection or through the APLL with a DCLK, ACLK, or CLK_UPSMP.

Direct ACLK Connection

1. Directly connect an external oscillator to either ACLK1 (Pin 26) or ACLK2 (Pin 27)
2. Select the pin with Register 0[4] SEL_MCLK_SRC.

Typical APLL Setup

Below are the typical steps for setting up the APLL as an MCLK source to the chip. For specific examples parts of this setup may change and are outlined in the following sections.

1. Enable Regulator and Low Noise Reference
    a. Register 138[0] PLL_REG_EN = 1'b1 (Enabled)
    b. Register 138[1] PLL_REG_LN = 1'b1 (Enabled)
2. Enable and select PLL Clock Input and MCLK source
    a. Register 136[5:4] SEL_PLL_CLK_IN = value
    b. Register 136[3] EN_PLL_CLK_IN = 1'b1 (Enable)
    c. Register 136[2] SEL_MCLK_IN_PLL = 1'b1 (PLL_CLK as MCLK)
3. Set required dividers for desired MCLK rate
    a. Register 142-143[3:0] PLL_CLK_IN_DIV = value
    b. Register 142-143[7:4] PLL_CLK_OUT_DIV = value
    c. Register 139-141[23:0] PLL_CLK_FB_DIV = value
    d. Register 138[7] PLL_FB_DIV_LOAD = 1'b0
    e. Register 138[7] PLL_FB_DIV_LOAD = 1'b1 (Load FB_DIV)
4. Enable the PLL Charge Pump, VCO, Circuitry, and Digital Core
    a. Register 137[3] PLL_CP_EN = 1'b1 (Enabled)
    b. Register 137[2] PLL_VCO_EN = 1'b1 (Enabled)
    c. Register 137[1] PLL_CLKSMP_EN = 1'b1 (Enabled)
    d. Register 137[0] PLL_DIG_RSTB = 1'b1 (Enabled)

DCLK Through APLL

This mode uses a DCLK input from the DATA_CLK pin (Pin 31) to generate an MCLK for the rest of the chip. To set up this configuration, follow the Typical APLL Setup and while replacing the below steps in setup.

2. Enable and select PLL Clock Input
    a. Register 136[5:4] SEL_PLL_CLK_IN = 2'b10 (DCLK)
    b. Register 136[3] EN_PLL_CLK_IN = 1'b1 (Enable)
    c. Register 136[2] SEL_MCLK_IN_PLL = 1'b1 (PLL_CLK as MCLK)

ACLK Through APLL (Related Base Rates)

This mode uses an ACLK input from either of the ACLK1/2 pins (Pins 26 & 27) to generate an MCLK for the rest of the chip. The input and output rates must have related base rates (i.e. 22.5792MHz↔45.1584MHz, 24.576MHz↔49.152MHz) To set up this configuration, follow the Typical APLL Setup and while replacing the below steps in setup.

2. Enable and select PLL Clock Input
    a. Register 136[5:4] SEL_PLL_CLK_IN = 2'b00 or 2'b01 (ACLK1 or ACLK2)
    b. Register 136[3] EN_PLL_CLK_IN = 1'b1 (Enable)
    c. Register 136[2] SEL_MCLK_IN_PLL = 1'b1 (PLL_CLK as MCLK)

ACLK Through APLL (Unrelated Base Rates)

This mode uses an ACLK input from either of the ACLK1/2 pins (Pins 26 & 27) to generate an MCLK for the rest of the chip. This mode supports unrelated base input and output rates (i.e. 22.5792MHz↔49.152MHz, 24.576MHz↔45.1584MHz) To set up this configuration, follow the Typical APLL Setup and while replacing the below steps in setup.

2. Enable and select PLL Clock Input
    a. Register 136[5:4] SEL_PLL_CLK_IN = 2'b00 or 2'b01 (ACLK1 or ACLK2)
    b. Register 136[3] EN_PLL_CLK_IN = 1'b1 (Enable)
    c. Register 136[2] SEL_MCLK_IN_PLL = 1'b1 (PLL_CLK as MCLK)
    d. Register 142-143[12] PLL_CLK_OUT_DIV_PHASE_EN = 1'b0 (Dynamic Tuning of Phase)

S/PDIF Frame Through Upsampler Through APLL

This mode uses CLK_UPSMP from the Upsampler as the input to the PLL.

2. Enable and select PLL Clock Input
    a. Register 136[5:4] SEL_PLL_CLK_IN = 2'b11 (CLK_UPSMP)
    b. Register 136[3] EN_PLL_CLK_IN = 1'b1 (Enable)
    c. Register 136[2] SEL_MCLK_IN_PLL = 1'b1 (PLL_CLK as MCLK)

Supply Modes

The ES9292PRO only supports 3 different supply modes with regards to AVCCH: Internal Fixed 2.85V, Internal Fixed 3.3V, and Internal Calibrated 3.3V. The power mode is determined by the state of two pins: AVCCH @ 3.3V or 4.5V and REXT pulldown state. Internal Calibrated mode uses an external resistor on Rext (Pin 11) and internal DAC resistors to normalize the DAC output.

Mode	AVCCH	REXT
Internal Fixed 2.85V	3.3V	NC
Internal Fixed 3.3V	4.5V	NC
Internal Calibrated 3.3V	4.5V	43.2kΩ to GND

Figure 29 - ES9292PRO Supply Modes

Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage • AVCC_3V3 • AVDD • AVCCH • VREF_BUF_ADC1/2 • VREF_BUF_DAC • DVDD	 • -0.3 to +3.7V with respect to ground • -0.3 to +3.7V with respect to ground • -0.3 to +4.75V with respect to ground • -0.3 to +3.7V with respect to ground • -0.3 to +3.7V with respect to ground • -0.3 to +1.4V with respect to ground
Storage Temperature	-65ºC to +150ºC
Operating Junction Temperature	+125ºC
Voltage Range for Digital Input Pins	-0.3V to AVDD (nom) +0.3V
Maximum/Minimum Input Voltage on IN_P IN_M pins	+6V to -0.4V

Table 37 - Absolute Maximum Ratings

WARNING: Stresses beyond those listed here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied.

ESD Ratings

ESD Standard	Rating
Human Body Model (HBM), ANSI/ESDA/JEDEC JS-001	2kV
Charge Device Model (CDM), ANSI/ESDA/JEDEC JS-002	500V

Table 38 - ESD Ratings

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

IO Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT
High-level input voltage	VIH	(AVDD / 2) + 0.2		V
Low-level input voltage	VIL		1.61	V
High-level output voltage	VOH	AVDD – 0.2		V
Low-level output voltage	VOL		0.2	V

Table 39 - I/O Electrical Characteristics

Switching Characteristics

Parameter	Notes	Min.	Typ.	Max.	Unit
MCLK[1]					
Frequency		22.5792	-	49.152	MHz
Duty Cycle		45	-	55	%
PCM Mode[2]					
WS Frequency (Word Select Clock)		MCLK/1024	-	MCLK/128	kHz
BCLK Frequency (Bit Clock)		(16*2*WS)	TDM_WORD_WIDTH)* (TDM_CH_NUM+1)*WS	MCLK	MHz
WS Frequency (Word Select Clock)	64FS Mode[3]	352.8	MCLK/64	768	kHz
BCLK Frequency (Bit Clock)		22.5792	MCLK	49.152	MHz
TDM Mode					
WS Frequency (Word Select Clock)	TDM4	MCLK/1024	-	MCLK/128	kHz
	TDM8		-	MCLK/256	kHz
	TDM16		-	MCLK/512	kHz
	TDM32		-	MCLK/1024	kHz
BCLK Frequency (Bit Clock)		(16*2*WS)	(TDM_WORD_WIDTH)* (TDM_CH_NUM+1)*WS	MCLK	MHz
DSD Mode					
DSD Clock Frequency		2.8224		MCLK/2	MHz

Table 40 - Switching Characteristics

[1] MCLK must be synchronous to the digital audio clock.

[2] In hardware mode, only 32-bit word widths are supported for both PCM, 32-bit and 16-bit for TDM.

[3] 64FS mode is for 705.6/768kHz with 45.1584/49.152MHz or 352.8/384kHz with 22.5792/24.576MHz.

Timing Characteristics

Bit-Clock (BCK) and Word-Select (WS) Timing

Master Mode

For maximum flexibility the Master BCK and WS generated can be inverted with Register 9[3] MASTER_WS_INVERT and Register 9[2] MASTER_DCLK_INVERT.

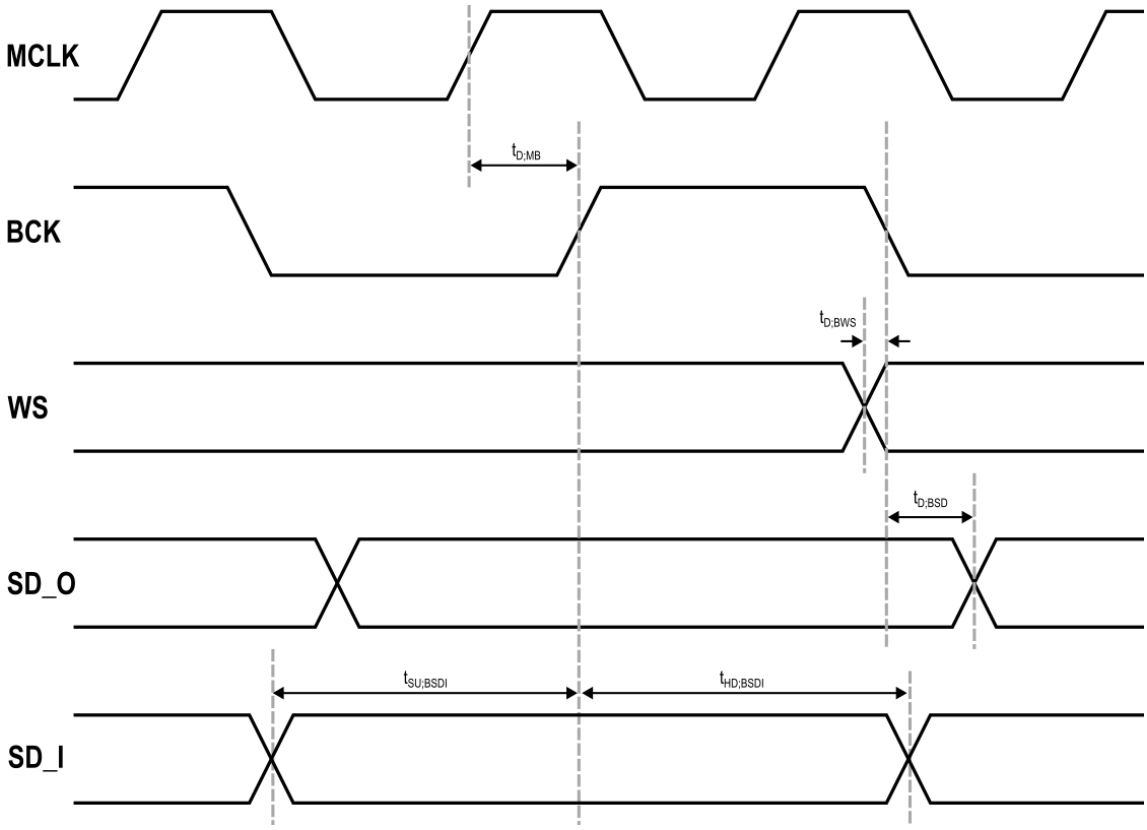


Figure 30 - Master Mode TDM Timing Diagrams

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK-to-BCK output delay	$t_{D;MB}$	6.58	-	17.99	ns
BCK-to-WS output delay	$t_{D;BWS}$	-1.34	-	3.44	ns
BCK-to-DATAx output delay	$t_{D;BSD}$	2.88	-	12.30	ns
BCK-to-SD_I setup time	$t_{SU;BSDI}$	-0.12	-	-	ns
BCK-to-SD_I hold time	$t_{HD;BSDI}$	0.38	-	-	ns

Figure 31 - Master Mode TDM Interface Timings

Slave Mode

In this diagram SD_O is the output data lines from the PDM/TDM Encoder and SD_I is the input data for the TDM Daisy Chain and the PCM/TDM Decoder.

For maximum flexibility the input Slave BCK can be inverted with Register 9[7] SLAVE_DCLK_INVERT.

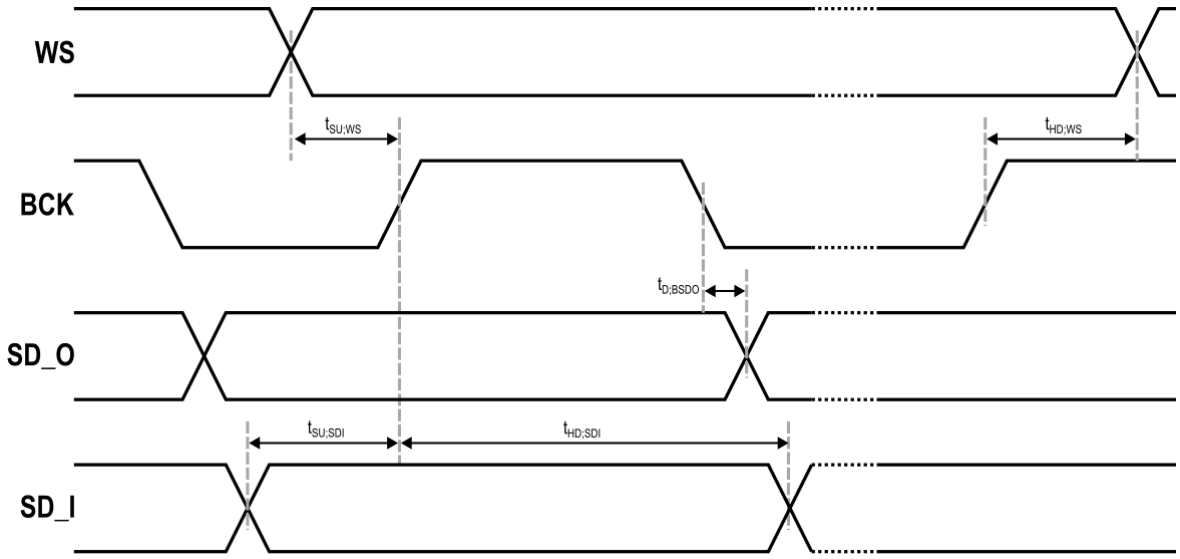


Figure 32 - Slave Mode TDM Timing Diagram

Parameter	Symbol	Min.	Typ.	Max.	Unit
WS setup time	$t_{SU;WS}$	-0.16	-	-	ns
WS hold time	$t_{HD;WS}$	0.63	-	-	ns
DATA Input setup time	$t_{SU;SDI}$	-0.12	-	-	ns
DATA Input hold time	$t_{HD;SDI}$	0.38	-	-	ns
BCK-to-DATAx output delay	$t_{D;BSDO}$	2.88	-	-	ns

Figure 33 - Slave Mode TDM Interface Timings

I²C Slave Interface Timing

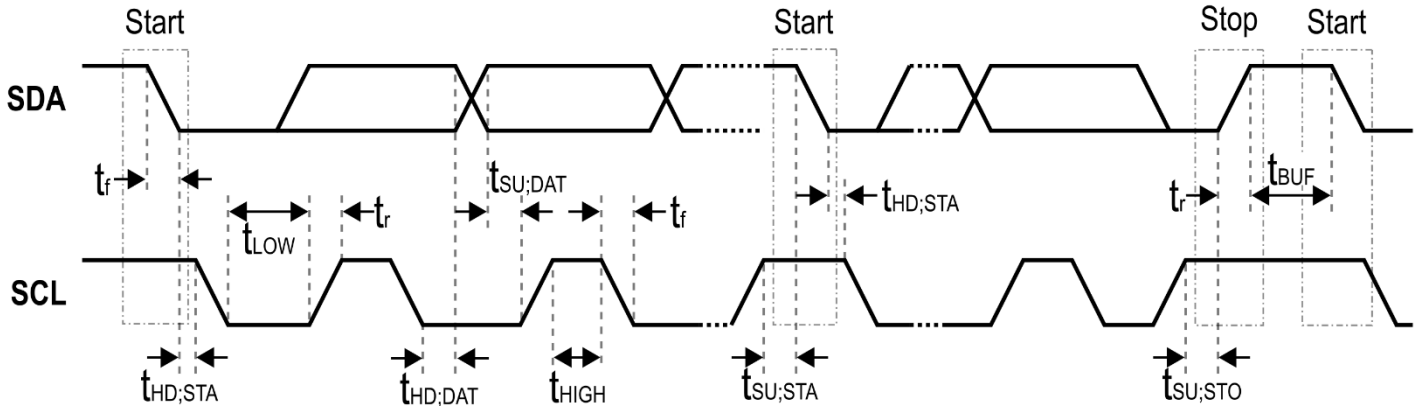


Figure 34 - I²C Slave Control Interface Timing

Parameter	Symbol	Standard-Mode		Fast-Mode		Fast-Mode Plus		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	0	100	0	400	0	1000	kHz
START condition hold time	$t_{HD;STA}$	4	-	0.6	-	0.26	-	us
LOW period of SCL	t_{LOW}	4.7	-	1.3	-	0.5	-	us
HIGH period of SCL (>10/CLK)	t_{HIGH}	4	-	0.6	-	0.26	-	us
START condition setup time (repeat)	$t_{SU;STA}$	4.7	-	0.6	-	0.26	-	us
SDA hold time from SCL falling	$t_{HD;DAT}$	0	-	0	-	0	-	us
SDA setup time from SCL rising	$t_{SU;DAT}$	250	-	100	-	50	-	ns
Rise time of SDA and SCL	t_r	-	1000	-	300		120	ns
Fall time of SDA and SCL	t_f	-	300	12	300	12	120	ns
STOP condition setup time	$t_{SU;STO}$	4	-	0.6	-	0.26	-	us
Bus free time between transmissions	t_{BUF}	4.7	-	1.3	-	0.5	-	us
Capacitive load for each bus line	C_b	-	400	-	400	-	550	pF

Table 41 - I²C Slave/Synchronous Slave Interface Timing Definitions

Note: It is recommended to use 2kΩ pull-up resistors on SDA and SCL. If the capacitive load on a bus line approaches its maximum value, a lower pull-up resistor value may need to be used.

SPI Slave Interface Timing

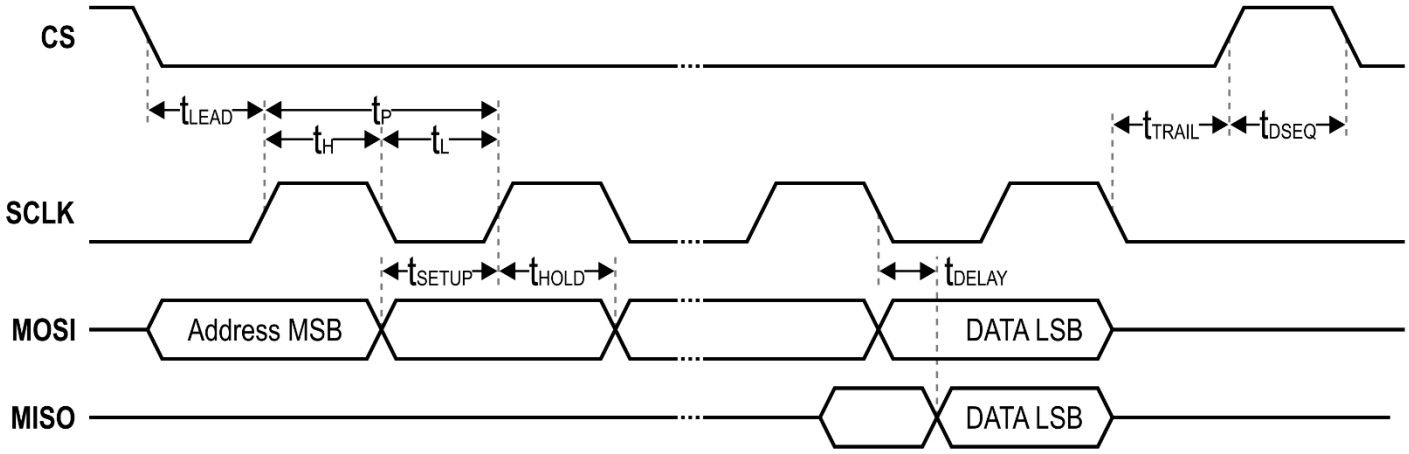


Figure 35 - SPI Slave Interface Timing

Parameter	Symbol	Min [ns]	Max [ns]
CS Lead Time (SCLK rising edge)	t_{LEAD}	2	-
CS Trail Time (SCLK falling edge)	t_{TRAIL}	2	-
MOSI Data Setup Time	t_{SETUP_MOSI}	5	-
MOSI Data Hold Time	t_{HOLD_MOSI}	7	-
SCLK-MISO Delay Time	t_{DELAY_MISO}	-	12
SCLK Period	t_{P_SCLK}	40	-
SCLK High Pulse Duration	t_{H_SCLK}	8	-
SCLK Low Pulse Duration	t_{L_SCLK}	8	-
Sequential Transfer Delay	t_{DSEQ}	40	-

Table 42 - SPI Slave Interface Timing

Recommended Operating Conditions

Table 43 shows the recommended operating conditions for the ES9292PRO.

PARAMETER	SYMBOL	CONDITIONS
Operating Temperature	T_A	-20°C to +85°C
AVCC_3V3		+3.3V ± 5%
AVDD		+3.3V ± 5%
AVCCH		+3.3V ± 5% or +4.5V ± 5%
DVDD		Internal +1.2V
VREF_BUF_ADC1/2		Internal +2.85V or Internal +3.3V
VREF_BUF_DAC		Internal +2.85V or Internal +3.3V
VREF_LN_ADC		Internal +2.85V
VREF_LN_DAC		Internal +2.85V
PLL_REG		Internal +2.65V
PLL_LN_REG		Internal +2.65V

Table 43 - Recommended Operating Conditions

Recommended Power Up Sequence

It is recommended for powering up that CHIP_EN remains low while the power supplies turn on.

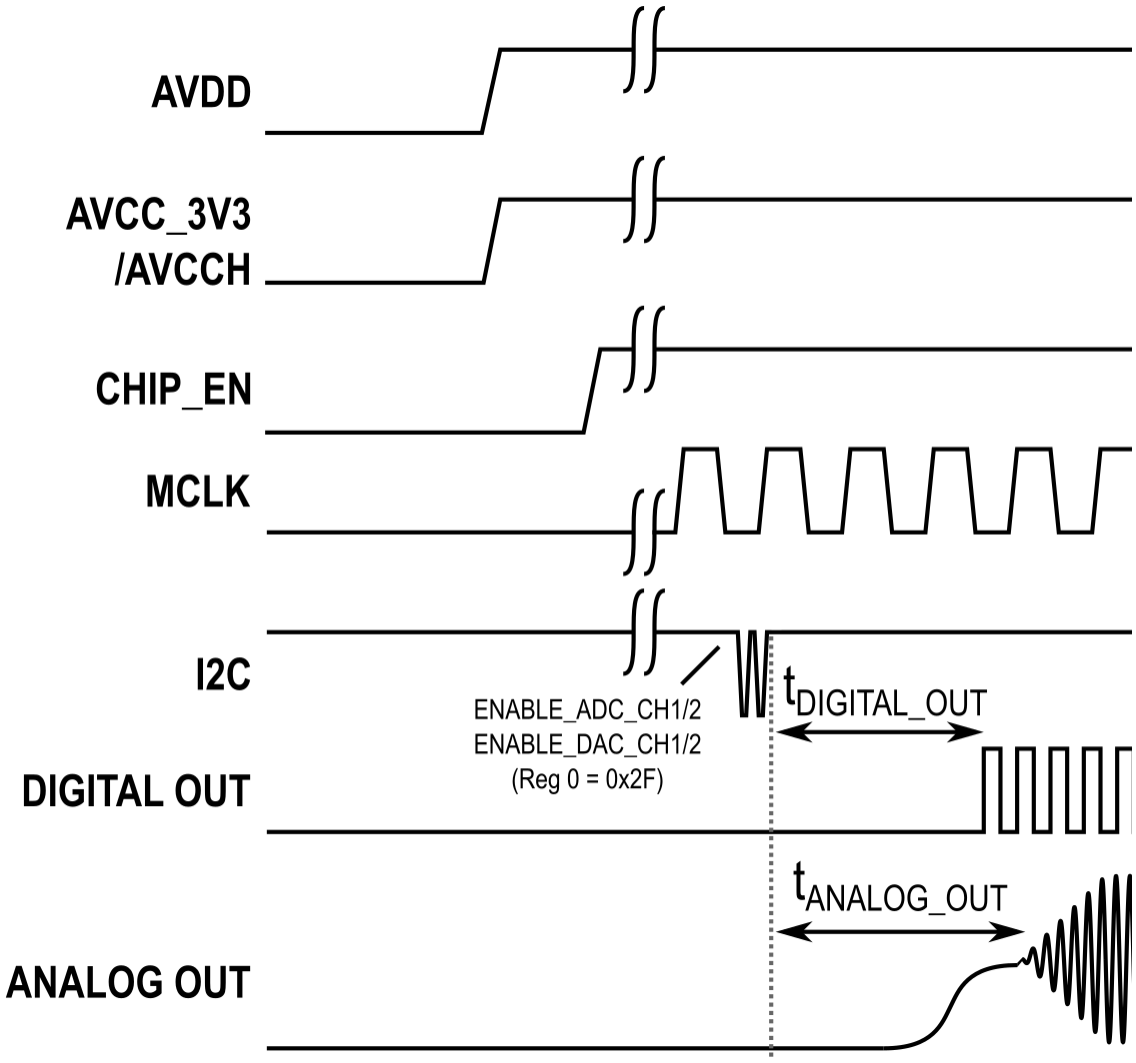


Figure 36 - Recommended Power Up Sequence

$$t_{digital\_out}[s] = \left(3 + \frac{900000}{2^{\sim MCLK\_24M\_DIV2}}\right) * \left(\frac{1}{MCLK}\right) \approx 18.3ms$$

$$t_{analog\_out}[s] = \left(2 + \frac{800000 + 2^{16+SOFT\_RAMP\_TIME}}{2^{\sim MCLK2\_24M\_DIV2}}\right) * \left(\frac{1}{MCLK}\right) + \frac{3}{FS} \approx 27ms\ @\ 48kHz$$

Power Consumption

Test Conditions (unless otherwise noted)
T_A = 25ºC, AVCC_3V3 = AVDD = +3.3V, AVCCH = +3.3V (Internal Fixed +2.85V Supply Mode)
ADC: 1.78Vrms Differential Input. DAC: 0dBFS Digital Input. AVDD supply includes DVDD current.
Automute Off, DC Block Off.

Parameter	Min	Typ.	Max	Unit
Standby (CHIP_EN=0)				
AVCC_3V3		<1		µA
AVCCH		<1		µA
AVDD		<1		µA

Parameter	Min	Typ.	Max	Unit
HW Mode 8 (I²S Slave 32-bit), MCLK = 24.576MHz				
AVCC_3V3		4.9		mA
AVCCH		42		mA
AVDD for 48kHz		20		mA
AVDD for 96kHz		25		mA
AVDD for 192kHz		33		mA
AVDD for 384kHz		30		mA

Note: Power consumption is from a sample size and is subject to change.

Performance

Test Conditions 1 (unless otherwise noted)
T_A = 25ºC, AVCC_3V3 = AVDD = 3.3V, AVCCH = +3.3V (Internal Fixed +2.85V) / +4.5V (Internal Fixed +3.3V), fs = 48kHz, HW mode, 49.152MHz clock, 1kHz input.

Note: Performance numbers were measured using the ESS ES9292PRO 1v0 evaluation board.

Parameter			Min	Typ.	Max	Unit
ADC Analog Input Characteristics						
Resolution					32	Bit
Differential Input Voltage (IN_P to IN_M)	0dBFS output			2		V_{rms}
Input DC Common Mode				VREF_BUF_ADC/2		V_{dc}
Stereo THD+N Ratio (+5dBV differential input, -1dBFS output)	fs=48kHz	BW=20Hz-20kHz		-118		dB
Stereo Dynamic Range (DNR) (2mVrms differential input, -60dBFS output)	Internal 2.85V	A-weighted		+128		dB
	Internal 3.3V			+128.5		dB
Input Impedance				260±15%		Ω

Table 44 - ES9292PRO ADC Performance

Parameter			Min	Typ.	Max	Unit
DAC Analog Output Characteristics						
Resolution					32	Bit
Output Voltage	0dBFS input			2		V_{rms}
Stereo THD+N Ratio (0dBFS input, differential output)	fs=48kHz BW=20Hz-20kHz	2Vrms,10kΩ		-118		dB
Stereo Dynamic Range (-60dBFS input, differential output)	Internal 2.85V	A-weighted		+128.5		dB
	Internal 3.3V			+130		dB
Output Impedance				390±15%		Ω

Table 45 - ES9292PRO DAC Performance

Register Overview

A system clock is not required to access registers.

Read/Write Register Addresses

Registers 0-199 (0x00 - 0xC7) are read and write registers.

Read-Only Register Addresses

Register 218-255 (0xDA - 0xFF) are read only registers.

Multi-Byte Registers

Multi-Byte registers must be written from LSB to MSB. Data is latched when MSB is written.
Multi-Byte registers must be read from LSB to MSB. Data is latched when LSB is read.
MSB is always stored in the highest register address.

Register Map

Addr (Hex)	Addr (Dec)	Register	7	6	5	4	3	2	1	0
0x00	0	SYS CONFIG	SOFT_RESET	RESERVED	EN_MCLK_IN	SEL_MCLK_SRC	ENABLE_DAC_CH2	ENABLE_DAC_CH1	ENABLE_ADC_CH2	ENABLE_ADC_CH1
0x01	1	FS CONFIG	RESERVED			ADC_MONO_MODE	RESERVED	ENABLE_64FS_MODE	AUTO_FS_DETECT_BLOCK_64FS	AUTO_FS_DETECT
0x02	2	ENCODER/DECODER CONFIG	ENABLE_PDM_DECODE	ENABLE_DSD_DECODE	ENABLE_DOP_DECODE	ENABLE_TDM_DECODE	ENABLE_PDM_ENCODE	ENABLE_DSD_ENCODE	ENABLE_DOP_ENCODE	ENABLE_TDM_ENCODE
0x03	3	OUTPUT SELECT	ENABLE_SPDIF_ENCODE	ENABLE_PDM_MIC_DECODE	RESERVED		OUTPUT_DATA_FORMAT_SEL			OUTPUT_FMT_FLW_INPUT
0x04	4	INPUT SELECT	ENABLE_SPDIF_DECODE	RESERVED			INPUT_DATA_FORMAT_SEL			AUTO_INPUT_FORMAT_SEL
0x05	5	FRONT-END CLOCK CONTROL	RESERVED	MCLK_128FS_HALF_DIV	MCLK_128FS_DIV					
0x06	6	BACK-END CLOCK CONTROL	RESERVED			MCLK_24M_DIV2	RESERVED			
0x07	7	MASTER CLK CONFIG	MASTER_DCLK_DIV							
0x08	8	MISC CLOCK CONFIG	RESERVED				ENABLE_WS_MONITOR	ENABLE_BCK_MONITOR	FORCE_PLL_LOCK	CLK_FAULT_DET_EN
0x09	9	MASTER MODE CONFIG	SLAVE_DCLK_INVERT	RESERVED	MASTER_WS_CLK_PHASE	MASTER_WS_PULSE_MODE	MASTER_WS_INVERT	MASTER_DCLK_INVERT	DSD_MASTER_MODE_EN	PCM_MASTER_MODE_EN
0x0A	10	TDM CONFIG 1	RESERVED	AUTO_CH_DETECT	RESERVED	TDM_CH_NUM				
0x0B	11	TDM CONFIG 2	RESERVED	NOISE_FLOOR_SHAPE_16BIT	TDM_WORD_WIDTH		TDM_BIT_DEPTH		TDM_VALID_EDGE	TDM_LJ
0x0C	12	TDM ENC SLOT CONFIG	RESERVED			TDM_ENC_SLOT_SEL_CH1				
0x0D	13		RESERVED			TDM_ENC_SLOT_SEL_CH2				
0x0E	14	TDM DEC SLOT CONFIG	RESERVED			TDM_DEC_SLOT_SEL_CH1				
0x0F	15		RESERVED			TDM_DEC_SLOT_SEL_CH2				
0x10	16	TDM ENC DAISY CHAIN	TDM_ENC_DAISY_CHAIN	RESERVED		TDM_ENC_DATA_LATCH_ADJ				
0x11	17	TDM DEC DAISY CHAIN	TDM_DEC_DAISY_CHAIN	RESERVED		TDM_DEC_DATA_LATCH_ADJ				
0x12	18	DSD MAPPING	RESERVED		DSD_ENC_LINE_SEL_CH2	DSD_ENC_LINE_SEL_CH1	RESERVED	DSD_ENC_DCLK_EDGE	DSD_DEC_CH_SEL_DATA3	DSD_DEC_CH_SEL_DATA2
0x13	19	PDM I/O CONFIG	RESERVED	PDM_DEC_SAMPLE_EDGE	PDM_DEC_DATA_PHASE	PDM_DEC_2X_GAIN_EN	RESERVED	PDM_ENC_SAMPLE_EDGE	PDM_ENC_DATA_PHASE	PDM_ENC_2X_GAIN_EN
0x14	20	PDM MIC CONFIG	RESERVED					PDM_MIC_SAMPLE_EDGE	PDM_MIC_DATA_PHASE	PDM_MIC_IN_SEL
0x15	21	PDM MIC CLK SELECT	RESERVED	MCLK_PDM_MIC_DIV						
0x16	22	S/PDIF ENCODER CONFIG	SPDIF_ENC_CS_WE	RESERVED	SPDIF_ENC_CS_BYTE_ADDR					SPDIF_ENC_DATA_SOURCE
0x17	23	S/PDIF ENCODER CS DATA	SPDIF_ENC_CS_BYTE_DATA							
0x18	24	S/PDIF DECODER CTRL	SPDIF_DEC_IN_SEL				SPDIF_DEC_PCM_LOOP	SPDIF_DEC_CH_SEL_CH2	SPDIF_DEC_CH_SEL_CH1	RESERVED
0x19	25	S/PDIF DECODER CONFIG	SPDIF_DEC_GLOBAL_IGNORE	SPDIF_DEC_IGNORE_VALID	SPDIF_DEC_IGNORE_DATA	SPDIF_DEC_PAYLOAD_BYTE_SEL				
0x1A	26	S/PDIF DECODER CS CONFIG	RESERVED							SPDIF_DEC_SUBFRAME_READ_SEL
0x1B	27	CLK UPSMP UCLK CONFIG	RESERVED							SEL_UCLK_SRC
0x1C	28	RESERVED	RESERVED							
0x1D	29	CLK UPSMP THRESHOLD	UPSMP_UCLK_THRESHOLD							
0x1E	30		RESERVED				UPSMP_UCLK_THRESHOLD			
0x1F-0x23	31-35	RESERVED	RESERVED							
0x24	36	VOLUME RAMP RATES	VOL_RAMP_RATE_UP							
0x25	37		VOL_RAMP_RATE_DOWN							
0x26	38	VOLUME RAMP SPEED	RESERVED							VOL_RAMP_SPEED_SEL
0x27-0x29	39-41	RESERVED	RESERVED							
0x2A	42	STATUS BITS MASK	MASK_DAC_ZCD_CH2	MASK_DAC_ZCD_CH1	MASK_ADC_ZCD_CH2	MASK_ADC_ZCD_CH1	MASK_ADC_OVERLOAD_CH2	MASK_ADC_OVERLOAD_CH1	MASK_PEAK_DET_CH2	MASK_PEAK_DET_CH1
0x2B	43	STATUS BITS CLEAR	CLEAR_DAC_ZCD_CH2	CLEAR_DAC_ZCD_CH1	CLEAR_ADC_ZCD_CH2	CLEAR_ADC_ZCD_CH1	CLEAR_ADC_OVERLOAD_CH2	CLEAR_ADC_OVERLOAD_CH1	CLEAR_PEAK_DET_CH2	CLEAR_PEAK_DET_CH1
0x2C-0x3C	44-60	RESERVED	RESERVED							
0x3D	61	GPIO1/2 CONFIG	GPIO2_CFG				GPIO1_CFG			
0x3E	62	GPIO3/4 CONFIG	GPIO4_CFG				GPIO3_CFG			
0x3F	63	GPIO5/6 CONFIG	GPIO6_CFG				GPIO5_CFG			
0x40	64	GPIO7/8 CONFIG	GPIO8_CFG				GPIO7_CFG			
0x41	65	GPIO9 CONFIG	RESERVED				GPIO9_CFG			

0x42	66	GPIO INPUT ENABLE	GPIO8_SDB	GPIO7_SDB	GPIO6_SDB	GPIO5_SDB	GPIO4_SDB	GPIO3_SDB	GPIO2_SDB	GPIO1_SDB
0x43	67		RESERVED							GPIO9_SDB
0x44	68	GPIO OUTPUT ENABLE	GPIO8_OE	GPIO7_OE	GPIO6_OE	GPIO5_OE	GPIO4_OE	GPIO3_OE	GPIO2_OE	GPIO1_OE
0x45	69		RESERVED							GPIO9_OE
0x46	70	GPIO INVERT	GPIO8_INV	GPIO7_INV	GPIO6_INV	GPIO5_INV	GPIO4_INV	GPIO3_INV	GPIO2_INV	GPIO1_INV
0x47	71		RESERVED							GPIO9_INV
0x48	72	GPIO WEAK KEEPER	GPIO8_WK_EN	GPIO7_WK_EN	GPIO6_WK_EN	GPIO5_WK_EN	GPIO4_WK_EN	GPIO3_WK_EN	GPIO2_WK_EN	GPIO1_WK_EN
0x49	73		RESERVED							GPIO9_WK_EN
0x4A	74	GPIO READ	GPIO8_READ	GPIO7_READ	GPIO6_READ	GPIO5_READ	GPIO4_READ	GPIO3_READ	GPIO2_READ	GPIO1_READ
0x4B	75		RESERVED							GPIO9_READ
0x4C	76	GPIO ADC FLAG CONFIG	RESERVED			ADC_LIVE_FLAG_EN	ADC_CH2_DET_FLAG_SEL		ADC_CH1_DET_FLAG_SEL	
0x4D	77	GPIO DAC FLAG CONFIG	RESERVED	DAC_FLAG_CH_SEL	GPIO_OR_SS_RAMP	GPIO_OR_AUTOMUTE	GPIO_OR_VOL_MIN	GPIO_AND_SS_RAMP	GPIO_AND_AUTOMUTE	GPIO_AND_VOL_MIN
0x4E	78	PWM COUNT	PWM_COUNT							
0x4F	79	PWM FREQUENCY	PWM_FREQ							
0x50	80		PWM_FREQ							
0x51	81	ADC NEGATION	RESERVED						ADC_NEG_SEL_CH2	ADC_NEG_SEL_CH1
0x52	82	ADC DATAPATH CONTROL	ADC_FILTER_SHAPE			ADC_BYPASS_FIR2X	ADC_BYPASS_FIR4X	ADC_BYPASS_IIR		
0x53	83	ADC FILTER CONFIG	RESERVED							
0x54	84		RESERVED		DC_BLOCK_EN_CH2	DC_BLOCK_EN_CH1	ADC_PROG_FIR_COEFF_WE	ADC_PROG_FIR_COEFF_EN	RESERVED	
0x55	85	ADC PROGRAM FIR ADDRESS	ADC_PROG_FIR_COEFF_STAGE	ADC_PROG_FIR_COEFF_ADDR						
0x56	86	ADC PROGRAM FIR DATA	ADC_PROG_FIR_COEFF_IN							
0x57	87		ADC_PROG_FIR_COEFF_IN							
0x58	88		ADC_PROG_FIR_COEFF_IN							
0x59	89	ADC VOLUME	ADC_VOLUME_CH1							
0x5A	90		ADC_VOLUME_CH2							
0x5B	91	ADC DIGITAL GAIN	RESERVED	ADC_DIGITAL_GAIN_CH2			RESERVED	ADC_DIGITAL_GAIN_CH1		
0x5C	92	ADC PHASE INVERSION	RESERVED						ADC_VOL_PHASE_INV_CH2	ADC_VOL_PHASE_INV_CH1
0x5D	93	ADC THD COMP	ADC_THD_COMP_C2							
0x5E	94		ADC_THD_COMP_C2							
0x5F	95		ADC_THD_COMP_C3							
0x60	96		ADC_THD_COMP_C3							
0x61	97	DETECTOR ENABLES	RESERVED		ADC_ZCD_EN_CH2	ADC_ZCD_EN_CH1	RESERVED		PEAK_DETECT_EN_CH2	PEAK_DETECT_EN_CH1
0x62	98	PEAK DETECT CONFIG	RESERVED	LOCK_PEAK_VALUE	RESERVED	PEAK_DECAY_RATE				
0x63	99	PEAK THRESHOLDS	PEAK_THRESH_CH1							
0x64	100		PEAK_THRESH_CH2							
0x65-0x68	101-104	RESERVED	RESERVED							
0x69	105	DAC FILTER CONFIG	DAC_PROG_FIR_COEFF_WE	DAC_PROG_FIR_COEFF_EN	DAC_BYPASS_IIR	DAC_BYPASS_FIR4X	DAC_BYPASS_FIR2X	DAC_FILTER_SHAPE		
0x6A	106	DAC PROGRAM FIR ADDRESS	DAC_PROG_FIR_COEFF_STAGE	DAC_PROG_FIR_COEFF_ADDR						
0x6B	107	DAC PROGRAM FIR DATA	DAC_PROG_FIR_COEFF_IN							
0x6C	108		DAC_PROG_FIR_COEFF_IN							
0x6D	109		DAC_PROG_FIR_COEFF_IN							
0x6E	110	DAC VOLUME	DAC_VOLUME_CH1							
0x6F	111		DAC_VOLUME_CH2							
0x70	112	DIRECT MONITOR VOLUME	DIR_MON_VOL_CH1							
0x71	113		DIR_MON_VOL_CH2							
0x72	114	DAC DIGITAL GAIN	RESERVED	DAC_DIGITAL_GAIN_CH2			RESERVED	DAC_DIGITAL_GAIN_CH1		
0x73	115	DAC PHASE INVERSION	DAC_ZCD_EN_CH2	DAC_ZCD_EN_CH1	DIR_MON_MONO_CH2	DIR_MON_MONO_CH1	DIR_MON_VOL_PHASE_INV_CH2	DIR_MON_VOL_PHASE_INV_CH1	DAC_VOL_PHASE_INV_CH2	DAC_VOL_PHASE_INV_CH1
0x74	116	DAC MUTE	RESERVED		DIR_MON_MUTE_CH2	DIR_MON_MUTE_CH1	RESERVED		DAC_MUTE_CH2	DAC_MUTE_CH1
0x75	117	SOFT RAMP CONFIG	RESERVED	DIR_MON_ADC_SEL	MUTE_RAMP_TO_GROUND	RESERVED	SOFT_RAMP_TIME			
0x76	118	DC OFFSET	DC_OFFSET_CH1							
0x77	119		DC_OFFSET_CH2							
0x78	120	AUTOMUTE ENABLE	RESERVED						AUTOMUTE_EN_CH2	AUTOMUTE_EN_CH1
0x79	121	AUTOMUTE CONFIG	AUTOMUTE_TIME							
0x7A	122		DSD_FAULT_DET_EN	DSD_DC_AM_EN	DSD_MUTE_AM_EN	RESERVED		AUTOMUTE_TIME		
0x7B	123	AUTOMUTE LEVEL	AUTOMUTE_LEVEL							
0x7C	124		AUTOMUTE_LEVEL							
0x7D	125		AUTOMUTE_OFF_LEVEL							
0x7E	126		AUTOMUTE_OFF_LEVEL							
0x7F	127	DAC THD COMP	DAC_THD_COMP_C2							
0x80	128		RESERVED				DAC_THD_COMP_C2			

0x81	129		DAC_THD_COMP_C3												
0x82	130		RESERVED							DAC_THD_COMP_C3					
0x83-0x87	131-135	RESERVED	RESERVED												
0x88	136	PLL CLOCK SELECT	RESERVED		PLL_CLK_PHASE_INV		SEL_PLL_CLK_IN			EN_PLL_CLK_IN		SEL_MCLK_IN_PLL		RESERVED	
0x89	137	PLL VCO & CP	RESERVED							PLL_CP_EN		PLL_VCO_EN		PLL_CLKSMP_EN	PLL_DIG_RSTB
0x8A	138	PLL REGULATOR	PLL_FB_DIV_LOAD		RESERVED									PLL_REG_LN	PLL_REG_EN
0x8B	139	PLL FEEDBACK DIV	PLL_CLK_FB_DIV												
0x8C	140		PLL_CLK_FB_DIV												
0x8D	141		PLL_CLK_FB_DIV												
0x8E	142	PLL IN & OUT DIV	PLL_CLK_OUT_DIV							PLL_CLK_IN_DIV					
0x8F	143		RESERVED						PLL_CLK_OUT_DIV_PHASE_EN	RESERVED					
0x90-0x92	144-146	RESERVED	RESERVED												
0x93	147	ASP CONTROL	ASP_DAC_CORE_EN		ASP_DAC_MEM_FLUSH		ASP_SPI_FLASH_REG_RUN		RESERVED	ASP_PROG_SOURCE_SEL		ASP_ADC_MEM_FLUSH		ASP_PROG_EN	ASP_ADC_CORE_EN
0x94	148	ASP BYPASS	RESERVED				ASP_DAC_BYPASS_CH2		ASP_DAC_BYPASS_CH1	RESERVED				ASP_ADC_BYPASS_CH2	ASP_ADC_BYPASS_CH1
0x95	149	RESERVED	RESERVED												
0x96	150	ASP PAIRED MODE	RESERVED				ASP_DAC_PAIRED_MODE		ASP_ADC_PAIRED_MODE	RESERVED				ASP_CORE_READ_SEL	
0x97	151	ASP INPUT3 SELECT	RESERVED				ASP_DAC_IN3_SEL_CH2		ASP_DAC_IN3_SEL_CH1	RESERVED				ASP_ADC_IN3_SEL_CH2	ASP_ADC_IN3_SEL_CH1
0x98	152	ASP PRAM WRITE EN	ASP_DAC_IN3_MIX_SEL		ASP_ADC_IN3_MIX_SEL		RESERVED							ASP_DAC_PRAM_WE	ASP_ADC_PRAM_WE
0x99	153	ASP COEFF DATA WRITE EN	RESERVED				ASP_DAC_COEFF_DATA_WE_CH2		ASP_DAC_COEFF_DATA_WE_CH1	RESERVED				ASP_ADC_COEFF_DATA_WE_CH2	ASP_ADC_COEFF_DATA_WE_CH1
0x9A	154	ASP PROG MEM ADDR	ASP_PROG_MEM_ADDR												
0x9B	155	ASP PROG MEM DATA	ASP_PROG_MEM_DATA												
0x9C	156		ASP_PROG_MEM_DATA												
0x9D	157		ASP_PROG_MEM_DATA												
0x9E	158		ASP_PROG_MEM_DATA												
0x9F	159	DMA DATA2	DMA_DATA2												
0xA0	160		DMA_DATA2												
0xA1	161		DMA_DATA2												
0xA2	162		DMA_DATA2												
0xA3	163	DMA DATA3	DMA_DATA3												
0xA4	164		DMA_DATA3												
0xA5	165		DMA_DATA3												
0xA6	166		DMA_DATA3												
0xA7	167	DMA DATA4	DMA_DATA4												
0xA8	168		DMA_DATA4												
0xA9	169		DMA_DATA4												
0xAA	170		DMA_DATA4												
0xAB	171	DMA DATA5	DMA_DATA5												
0xAC	172		DMA_DATA5												
0xAD	173		DMA_DATA5												
0xAE	174		DMA_DATA5												
0xAF	175	DMA DATA6	DMA_DATA6												
0xB0	176		DMA_DATA6												
0xB1	177		DMA_DATA6												
0xB2	178		DMA_DATA6												
0xB3	179	DMA DATA7	DMA_DATA7												
0xB4	180		DMA_DATA7												
0xB5	181		DMA_DATA7												
0xB6	182		DMA_DATA7												
0xB7	183	DMA DATA8	DMA_DATA8												
0xB8	184		DMA_DATA8												
0xB9	185		DMA_DATA8												
0xBA	186		DMA_DATA8												
0xBB	187	DMA CORE MASK	RESERVED				DMA_DAC_CORE_MASK_CH2		DMA_DAC_CORE_MASK_CH1	RESERVED				DMA_ADC_CORE_MASK_CH2	DMA_ADC_CORE_MASK_CH1
0xBC	188	DMA WRITE EN	DMA_DATA8_WE		DMA_DATA7_WE		DMA_DATA6_WE		DMA_DATA5_WE	DMA_DATA4_WE		DMA_DATA3_WE		DMA_DATA2_WE	DMA_DATA1_WE
0xBD-0xC5	189-197	RESERVED	RESERVED												
0xC6	198	SPI MASTER CONFIG	SPI_M_PULSE_WIDTH							SPI_M_EN		SPI_M_MODE		SPI_M_SEND_BYTE	SPI_M_START
0xC7	199	SPI MASTER DATA OUT	SPI_M_DATA_O												
0xDA	218	OUTPUT FMT VALIDITY READ	RESERVED							OUTPUT_DATA_FORMAT_SEL_OVR					TDM_ENC_VALID
0xDB	219	INPUT FMT VALIDITY READ	PLL_LOCKED		INPUT_DATA_FORMAT_SEL_OVR					UPSMP_LOCK		SPDIF_DEC_VALID		DOP_DEC_VALID	TDM_DEC_VALID

0xDC	220	AUTO FS READ	EN_64FS_MODE_AUTO	MCLK_128FS_HALF_DIV_AUTO	MCLK_128FS_DIV_AUTO					
0xDD	221	CLOCK VALIDITY	RATIO_VALID	BCK_INVALID	WS_INVALID	AUTO_CH_NUM				
0xDE	222	S/PDIF DATA READ	SPDIF_DEC_DATA_READ							
0xDF-0xE0	223-224	RESERVED	RESERVED							
0xE1	225	CHIP ID	CHIP_ID							
0xE2-0xE5	226-229	RESERVED	RESERVED							
0xE6	230	GPIO READBACK	GPIO8_R	GPIO7_R	GPIO6_R	GPIO5_R	GPIO4_R	GPIO3_R	GPIO2_R	GPIO1_R
0xE7	231		RESERVED							GPIO9_R
0xE8	232	ADC CLIP DETECT FLAGS	ADC_OVERLOAD_FLAG_LAT_CH2	ADC_OVERLOAD_FLAG_LAT_CH1	ADC_OVERLOAD_FLAG_CH2	ADC_OVERLOAD_FLAG_CH1	PEAK_FLAG_LAT_CH2	PEAK_FLAG_LAT_CH1	PEAK_FLAG_CH2	PEAK_FLAG_CH1
0xE9	233	ADC ZERO CROSS FLAGS	RESERVED				ADC_ZERO_CROSS_LAT_CH2	ADC_ZERO_CROSS_LAT_CH1	ADC_ZERO_CROSS_CH2	ADC_ZERO_CROSS_CH1
0xEA	234	PEAK READ	PEAK_LEVEL_CH1							
0xEB	235		PEAK_LEVEL_CH1							
0xEC	236		PEAK_LEVEL_CH2							
0xED	237		PEAK_LEVEL_CH2							
0xEE	238	ADC PROG FIR COEFF OUT READ	PROG_FIR_COEFF_OUT_ADC							
0xEF	239		PROG_FIR_COEFF_OUT_ADC							
0xF0	240		PROG_FIR_COEFF_OUT_ADC							
0xF1	241	DAC LIVE STATUS FLAGS	SS_RAMP_DOWN_CH2	SS_RAMP_DOWN_CH1	SS_RAMP_UP_CH2	SS_RAMP_UP_CH1	AUTOMUTE_CH2	AUTOMUTE_CH1	VOL_MIN_CH2	VOL_MIN_CH1
0xF2	242	DAC ZERO CROSS FLAGS	RESERVED				DAC_ZERO_CROSS_LAT_CH2	DAC_ZERO_CROSS_LAT_CH1	DAC_ZERO_CROSS_CH2	DAC_ZERO_CROSS_CH1
0xF3	243	DAC PROG FIR COEFF OUT READ	PROG_FIR_COEFF_OUT_DAC							
0xF4	244		PROG_FIR_COEFF_OUT_DAC							
0xF5	245		PROG_FIR_COEFF_OUT_DAC							
0xF6-0xF7	246-247	RESERVED	RESERVED							
0xF8	248	SPI MASTER BUSY	SPI_M_ASP_PROG_BUSY	RESERVED		SPI_M_FULL_BYTE	RESERVED			
0xF9-0xFA	249-250	RESERVED	RESERVED							
0xFB	251	ASP CORE OUTPUT2	ASP_OUT2_READ							
0xFC	252		ASP_OUT2_READ							
0xFD	253		ASP_OUT2_READ							
0xFE	254	RESERVED	RESERVED							
0xFF	255	SPI MASTER DATA IN	SPI_M_DATA_I							

Table 46 - Register Map

Register Listing

System Registers

Register 0: SYS CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b1	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RESET	Performs soft reset to digital core, resetting registers to their power-on defaults.
[6]	RESERVED	N/A
[5]	EN_MCLK_IN	Enables clock inputs to the digital core. • 1'b0: Disabled • 1'b1: Enabled (default)
[4]	SEL_MCLK_SRC	Selects digital core and ADC clock source when EN_MCLK_IN is set. • 1'b0: ACLK1 (default) • 1'b1: ACLK2
[3]	ENABLE_DAC_CH2	Enables the DAC CH2 interpolation path. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	ENABLE_DAC_CH1	Enables the DAC CH1 interpolation path. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	ENABLE_ADC_CH2	Enables the ADC CH2 decimation path. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ENABLE_ADC_CH1	Enables the ADC CH1 decimation path. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 1: FS CONFIG

Bits	[7:5]	[4]	[3]	[2]	[1]	[0]
Default	3'b000	1'b0	1'd0	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4]	ADC_MONO_MODE	Enables ADC mono mode, summing CH1 and CH2 onto the CH1 path. • 1'b0: Disabled (default) • 1'b1: Enabled
[3]	RESERVED	N/A
[2]	ENABLE_64FS_MODE	Enables 64FS mode for 768k sample rate. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	AUTO_FS_DETECT_BLOCK_64FS	Block AUTO_FS_DETECT from transitioning to 64FS mode when the detected MCLK/MCLK_128FS ratio is 64. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	AUTO_FS_DETECT	Automatically determine optimal MCLK/MCLK_128FS ratio, from detected FS. • 1'b0: Disabled, use MCLK_128FS_DIV to set ratio. • 1'b1: Enabled, overrides MCLK_128FS_DIV (default)

Register 2: ENCODER/DECODER CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b1	1'b0	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7]	ENABLE_PDM_DECODE	Enables PDM decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	ENABLE_DSD_DECODE	Enables DSD decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[5]	ENABLE_DOP_DECODE	Enables DoP decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[4]	ENABLE_TDM_DECODE	Enables the PCM/TDM decoding clock. • 1'b0: Disabled • 1'b1: Enabled (default)
[3]	ENABLE_PDM_ENCODE	Enables PDM encoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	ENABLE_DSD_ENCODE	Enables DSD encoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	ENABLE_DOP_ENCODE	Enables DoP encoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ENABLE_TDM_ENCODE	Enables the PCM/TDM encoding clock. • 1'b0: Disabled • 1'b1: Enabled (default)

Register 3: OUTPUT SELECT

Bits	[7]	[6]	[5:4]	[3:1]	[0]
Default	1'b0	1'b0	2'd0	3'b000	1'b0

Bits	Mnemonic	Description
[7]	ENABLE_SPDIF_ENCODE	Enables the S/PDIF encoding clock. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	ENABLE_PDM_MIC_DECODE	Enables PDM microphone decoding clock. • 1'b0: Disabled (default) • 1'b1: Enabled
[5:4]	RESERVED	N/A
[3:1]	OUTPUT_DATA_FORMAT_SEL	Select which digital output to use. • 3'b000: PCM/TDM (default) • 3'b001: DoP • 3'b010: DSD • 3'b011: PDM • 3'b100: S/PDIF • 3'b101: DoPoS • Others: Reserved
[0]	OUTPUT_FMT_FLW_INPUT	Configure the output data format to follow the input data format. • 1'b0: Output data format is set by OUTPUT_DATA_FMT_SEL (default) • 1'b1: Output data format is tied to the input data format (auto if applicable) Note: AUTO_FORMAT_SEL cannot select PDM format.

Register 4: INPUT SELECT

Bits	[7]	[6:4]	[3:1]	[0]
Default	1'b0	3'd0	3'b000	1'b0

Bits	Mnemonic	Description
[7]	ENABLE_SPDIF_DECODE	Enables the S/PDIF decoding clock. • 1'b0: Disabled (default) • 1'b1: Enabled
[6:4]	RESERVED	N/A
[3:1]	INPUT_DATA_FORMAT_SEL	Select which digital input to use. • 3'b000: PCM/TDM (default) • 3'b001: DoP • 3'b010: DSD • 3'b011: PDM • 3'b100: S/PDIF • 3'b101: DoPoS • Others: Reserved
[0]	AUTO_INPUT_FORMAT_SEL	Automatic input data format selection config. • 1'b0: Disables auto input format select. Input data format set by INPUT_DATA_FORMAT_SEL (default) • 1'b1: Automatically determine the input data format. Note: AUTO_INPUT_FORMAT_SEL cannot select PDM format.

Register 5: FRONT-END CLOCK CONTROL

Bits	[7]	[6]	[5:0]
Default	1'd0	1'b0	6'd3

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	MCLK_128FS_HALF_DIV	• 1'b0: Divide by SELECT_ADC_NUM + 1 (default) • 1'b1: Divide by half of SELECT_ADC_NUM + 1 Note: Can only produce half of an odd number divide
[5:0]	MCLK_128FS_DIV	Whole number divide value + 1 for MCLK_128FS (MCLK/divide_value). • 6'd0: Whole number divide value + 1 = 1 • 6'd3: Whole number divide value + 1 = 4 (default)

Register 6: BACK-END CLOCK CONTROL

Bits	[7:5]	[4]	[3:0]
Default	3'b000	1'b0	4'b1000

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4]	MCLK_24M_DIV2	Sets the rate of internal clocks, relative to MCLK. For the ADC, determines MCLK_24M and ADC_CLK, both must be 22.5792MHz or 24.576MHz. For the DAC, determines scaling factor to maintain consistency across MCLKs. • 1'b0: Rate = MCLK (default) • 1'b1: Rate = MCLK/2
[3:0]	RESERVED	N/A

Register 7: MASTER CLK CONFIG

Bits	[7:0]
Default	8'd7

Bits	Mnemonic	Description
[7:0]	MASTER_DCLK_DIV	Master mode DCLK and WS generation clock divider. Whole number divide value + 1 for CLK_BCK_WS_GEN (MCLK/divide_value).

Register 8: MISC CLOCK CONFIG

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	4'b0000	1'b1	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	ENABLE_WS_MONITOR	Enable WS monitor, used to detect the validity of the WS signal. WS is considered invalid if BCK/WS > 1024. • 1'b0: Disabled • 1'b1: Enabled (default)
[2]	ENABLE_BCK_MONITOR	Enable BCK monitor, used to detect the validity of the BCK signal. BCK is considered invalid if MCLK/BCK > 256. • 1'b0: Disabled • 1'b1: Enabled (default)
[1]	FORCE_PLL_LOCK	Clock locking status control with PLL_LOCKED. • 1'b0: clock locking status is determined by PLL_LOCKED • 1'b1: Ignore PLL_LOCKED signal, set lock status to 1'b1
[0]	CLK_FAULT_DET_EN	Enable the clock detection circuit, sets the CLK_AVALID signal. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 9: MASTER MODE CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'd0	1'b1	1'b0	1'b0	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SLAVE_DCLK_INVERT	Inverts the DCLK input on DATA_CLK. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[6]	RESERVED	N/A
[5]	MASTER_WS_CLK_PHASE	Determines the CLK_BCK edge DATA_WS (GPIO2) is output on, in master mode. • 1'b0: Negative edge • 1'b1: Positive edge (default) Note: MASTER_BCK_INVERT inverts this logic.
[4]	MASTER_WS_PULSE_MODE	When enabled, master WS is a 1 BCK pulse signal instead of a 50% duty cycle signal. • 1'b0: 50% duty cycle WS signal (default) • 1'b1: Pulse WS signal
[3]	MASTER_WS_INVERT	Inverts master WS output on DATA1. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[2]	MASTER_DCLK_INVERT	Inverts master DCLK output on DATA_CLK. • 1'b0: Non-inverted • 1'b1: Inverted (default)
[1]	DSD_MASTER_MODE_EN	Enables DSD master mode, generating DCLK. • 1'b0: Disabled, slave mode (default) • 1'b1: Enabled
[0]	PCM_MASTER_MODE_EN	Enables PCM master mode, generating BCK and WS. • 1'b0: Disabled, slave mode (default) • 1'b1: Enabled

Register 10: TDM CONFIG 1

Bits	[7]	[6]	[5]	[4:0]
Default	1'b0	1'b0	1'b0	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	AUTO_CH_DETECT	Automatically determine the number of TDM channels in a sample, based on the BCK/WS ratio. • 1'b0: Disabled, use TDM_CH_NUM to set channels (default) • 1'b1: Enabled, overrides TDM_CH_NUM Note: Only active in TDM slave mode.
[5]	RESERVED	N/A
[4:0]	TDM_CH_NUM	Sets number of channels in each frame. • 5'd0: 1 channel • 5'd1: 2 channels (default) • 5'd31: 32 channels

Register 11: TDM CONFIG 2

Bits	[7]	[6]	[5:4]	[3:2]	[1]	[0]
Default	1'd0	1'b0	2'b00	2'b00	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	NOISE_FLOOR_SHAPE_16BIT	Sets the shape of the 16-bit PCM/TDM noise floor. • 1'b0: 1st order shaping (default) • 1'b1: Flat shaping
[5:4]	TDM_WORD_WIDTH	Sets the width, in bits, of one data word / subframe. A subframe is a frame divided by the number of channels. • 2'b00: 32-bits (default) • 2'b01: 24-bits • 2'b10: 16-bits
[3:2]	TDM_BIT_DEPTH	Sets the bit depth, number of data bits, in one data word / subframe. • 2'b00: 32-bit (default) • 2'b01: 24-bit • 2'b10: 16-bit
[1]	TDM_VALID_EDGE	Sets which WS edge the frame starts on. • 1'b0: Frame starts on negedge of WS (default) • 1'b1: Frame starts on posedge of WS
[0]	TDM_LJ	Sets left-justified mode. • 1'b0: One BCK period delay (default) • 1'b1: Left-justified

Register 13-12: TDM ENC SLOT CONFIG

Bits	[15:13]	[12:8]	[7:5]	[4:0]
Default	3'd0	5'd1	3'd0	5'd0

Bits	Mnemonic	Description
[15:13]	RESERVED	N/A
[12:8]	TDM_ENC_SLOT_SEL_CH2	Selects which TDM channel slot is filled by the CH2 data. • 5'd0: Slot 1 • 5'd1: Slot 2 (default) • 5'd31: Slot 32
[7:5]	RESERVED	N/A
[4:0]	TDM_ENC_SLOT_SEL_CH1	Selects which TDM channel slot is filled by the CH1 data. • 5'd0: Slot 1 (default) • 5'd31: Slot 32

Register 15-14: TDM DEC SLOT CONFIG

Bits	[15:13]	[12:8]	[7:5]	[4:0]
Default	3'd0	5'd1	3'd0	5'd0

Bits	Mnemonic	Description
[15:13]	RESERVED	N/A
[12:8]	TDM_DEC_SLOT_SEL_CH2	Selects which TDM channel slot is latched into CH2. • 5'd0: Slot 1 • 5'd1: Slot 2 (default) • 5'd31: Slot 32
[7:5]	RESERVED	N/A
[4:0]	TDM_DEC_SLOT_SEL_CH1	Selects which TDM channel slot is latched into CH1. • 5'd0: Slot 1 (default) • 5'd31: Slot 32

Register 16: TDM ENC DAISY CHAIN

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	TDM_ENC_DAISY_CHAIN	Enables TDM encoder daisy chain mode. • 1'b0: Disabled (default) • 1'b1: Enabled
[6:5]	RESERVED	N/A
[4:0]	TDM_ENC_DATA_LATCH_ADJ	Adjusts the position of the MSB within each TDM slot by TDM_ENC_DATA_LATCH_ADJ clock cycles. • 5'd0: Normal position • 5'd1-31: Data output TDM_ENC_DATA_LATCH_ADJ BCKs early

Register 17: TDM DEC DAISY CHAIN

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	TDM_DEC_DAISY_CHAIN	Enables TDM decoder daisy chain mode. • 1'b0: Disabled (default) • 1'b1: Enabled
[6:5]	RESERVED	N/A
[4:0]	TDM_DEC_DATA_LATCH_ADJ	Adjusts the position of the MSB within each TDM slot by TDM_DEC_DATA_LATCH_ADJ clock cycles. DAC data sampling is delayed from the normal position. • 5'd0: Normal position • 5'd1-31: DAC_TDM_DATA_LATCH_ADJ BCKs delay before sampling data

Register 18: DSD MAPPING

Bits	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	2'd0	1'b1	1'b0	1'd0	1'b0	1'b1	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	DSD_ENC_LINE_SEL_CH2	DSD Encoder Data Line assigned to CH1 • 1'b0: DATA4 (default) • 1'b1: DATA5
[4]	DSD_ENC_LINE_SEL_CH1	DSD Encoder Data Line assigned to CH2 • 1'b0: DATA4 • 1'b1: DATA5 (defaullt)
[3]	RESERVED	N/A
[2]	DSD_ENC_DCLK_EDGE	Selects the DCLK edge the DSD data is output on • 1'b0: Negedge (default) • 1'b1: Posedge
[1]	DSD_DEC_CH_SEL_DATA3	DSD Encoder channel data assigned to DATA3 • 1'b0: CH1 • 1'b1: CH2 (default)
[0]	DSD_DEC_CH_SEL_DATA2	DSD Encoder channel data assigned to DATA2 • 1'b0: CH1 (defaullt) • 1'b1: CH2

Register 19: PDM I/O CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'd0	1'b1	1'b0	1'b0	1'd0	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	PDM_DEC_SAMPLE_EDGE	Sets the edge of DATA_CLK where the PDM sample increments. • 1'b0: Rising edge • 1'b1: Falling edge (default)
[5]	PDM_DEC_DATA_PHASE	Selects the CH input edges of the PDM decoder. • 1'b0: CH1 on the rising edge of DATA_CLK, CH2 on the falling edge (default) • 1'b1: CH2 on the rising edge of DATA_CLK, CH1 on the falling edge
[4]	PDM_DEC_2X_GAIN_EN	Sets the overall datapath gain of the PDM decoder path. • 1'b0: 1x gain (default) • 1'b1: 2x gain
[3]	RESERVED	N/A
[2]	PDM_ENC_SAMPLE_EDGE	Sets the edge of DATA_CLK where the PDM sample increments. • 1'b0: Rising edge • 1'b1: Falling edge (default)
[1]	PDM_ENC_DATA_PHASE	Selects the CH output edges of the PDM encoder. • 1'b0: CH1 on the rising edge of DATA_CLK, CH2 on the falling edge (default) • 1'b1: CH2 on the rising edge of DATA_CLK, CH1 on the falling edge
[0]	PDM_ENC_2X_GAIN_EN	Sets the overall datapath gain of the PDM encoder path. • 1'b0: 1x gain (default) • 1'b1: 2x gain

Register 20: PDM MIC CONFIG

Bits	[7:3]	[2]	[1]	[0]
Default	5'd0	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7:3]	RESERVED	N/A
[2]	PDM_MIC_SAMPLE_EDGE	Sets the edge of PDM_CLK where the PDM sample increments. • 1'b0: Rising edge • 1'b1: Falling edge (default)
[1]	PDM_MIC_DATA_PHASE	Selects the CH output edges of the PDM Mic Decoder • 1'b0: CH1 on the rising edge of DCLK, CH2 on the falling edge (default) • 1'b1: CH2 on the rising edge of DCLK, CH1 on the falling edge
[0]	PDM_MIC_IN_SEL	Selects the input to the ADC datapath. • 1'b0: Analog input to datapath (default) • 1'b1: PDM input to datapath

Register 21: PDM MIC CLK SELECT

Bits	[7]	[6:0]
Default	1'b0	7'd3

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:0]	MCLK_PDM_MIC_DIV	Frequency divider for the PDM microphone clock, PDM_CLK. Overidden by AUTO_FS_DETECT, sets PDM_CLK_DIV = MCLK_128FS_DIV_AUTO[3:0]. • 7'd0: 2 * (PDM_CLK_DIV + 1) = DIV2 • 7'd3: 2 * (PDM_CLK_DIV + 1) = DIV8 (default) $\text{PDM\_CLK [Hz]} = \frac{\text{MCLK}}{2 \cdot (\text{PDM\_CLK\_DIV} + 1)}$

Register 22: S/PDIF ENCODER CONFIG

Bits	[7]	[6]	[5:1]	[0]
Default	1'b0	1'b0	5'd0	1'b0

Bits	Mnemonic	Description
[7]	SPDIF_ENC_CS_WE	Write enable for the S/PDIF channel status bits. Writes the SPDIF_CS_DATA to the byte at address SPDIF_CS_BYTE_SEL. Toggle high-low to perform a write.
[6]	RESERVED	N/A
[5:1]	SPDIF_ENC_CS_BYTE_ADDR	Byte of the 192-bit S/PDIF Channel Status to write to.
[0]	SPDIF_ENC_DATA_SOURCE	Selects the data source for the S/PDIF encoder. • 1'b0: Output of the ADC datapath (default) • 1'b1: Output of the TDM decoder Note: The TDM decoder output is bit perfect.

Register 23: S/PDIF ENCODER CS DATA

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	SPDIF_ENC_CS_BYTE_DATA	Data to write into the 192-bit S/PDIF Channel Status.

Register 24: S/PDIF DECODER CTRL

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	4'd0	1'b0	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7:4]	SPDIF_DEC_IN_SEL	Selects the S/PDIF Decoder data input pin. • 4'd0: Disconnected (default) • 4'd1: DATA1 • 4'd3: DATA3 • 4'd5: DATA5 • 4'd6: GPIO3 • 4'd7: GPIO4 • 4'd8: GPIO5 • 4'd9: GPIO6 • 4'd10: GPIO7 • 4'd11: GPIO8 • 4'd12: GPIO9 • Others: Reserved Note: GPIOx pins also require the GPIOx_SDB to be enabled.
[3]	SPDIF_DEC_PCM_LOOP	Connects the S/PDIF decoder output to the ADC PCM datapath, overriding ADC data. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	SPDIF_DEC_CH_SEL_CH2	S/PDIF subframe data assigned to CH2. • 1'b0: Subframe A • 1'b1: Subframe B (default)
[1]	SPDIF_DEC_CH_SEL_CH1	S/PDIF subframe data assigned to CH1. • 1'b0: Subframe A (default) • 1'b1: Subframe B
[0]	RESERVED	N/A

Register 25: S/PDIF DECODER CONFIG

Bits	[7]	[6]	[5]	[4:0]
Default	1'b1	1'b0	1'b0	5'd0

Bits	Mnemonic	Description
[7]	SPDIF_DEC_GLOBAL_IGNORE	Sets the S/PDIF validity flag and data field to effect all channels globally. • 1'b0: Disabled, validity and data only effect their respective channel. • 1'b1: Enabled (default)
[6]	SPDIF_DEC_IGNORE_VALID	Ignore the S/PDIF validity flag in time slot 28 of the subframe. • 1'b0: Disabled, Mute the S/PDIF output(s) (default) • 1'b1: Ignore the validity flag, assume valid S/PDIF
[5]	SPDIF_DEC_IGNORE_DATA	Ignore the data field in channel status Byte 0[1] when it is set to "non-audio". • 1'b0: Disabled, mute the S/PDIF output(s) (default) • 1'b1: Ignore the data field, assume audio S/PDIF
[4:0]	SPDIF_DEC_PAYLOAD_BYTE_SEL	Selects the byte of the S/PDIF decoder payload in register 222 SPDIF_DEC_PAYLOAD_READ.

Register 26: S/PDIF DECODER CS CONFIG

Bits	[7:1]	[0]
Default	7'b1100100	1'b0

Bits	Mnemonic	Description
[7:1]	RESERVED	N/A
[0]	SPDIF_DEC_SUBFRAME_READ_SEL	Selects which subframe the status bits are read from • 1'b0: Subframe A (default) • 1'b1: Subframe B

Register 27: CLK UPSMP UCLK CONFIG

Bits	[7:1]	[0]
Default	7'b0000000	1'b0

Bits	Mnemonic	Description
[7:1]	RESERVED	N/A
[0]	SEL_UCLK_SRC	Selects the clock pin to be the source of UCLK. Requires the PLL_CLK source to be CLK_UPSMP. • 1'b0: ACLK1 (default) • 1'b1: ACLK2

Register 28: RESERVED

Register 30-29: CLK UPSMP THRESHOLD

Bits	[15:12]	[11:0]
Default	4'd0	12'd2000

Bits	Mnemonic	Description
[15:12]	RESERVED	N/A
[11:0]	UPSMP_UCLK_THRESHOLD	UCLK threshold for FS detection Upsampler operation. $$\text{Threshold} = 2000 \cdot \frac{\text{UCLK [MHz]}}{50\ \text{[MHz]}}$$

Register 35-31: RESERVED

Register 37-36: VOLUME RAMP RATES

Bits	[15:8]	[7:0]
Default	8'h20	8'h20

Bits	Mnemonic	Description
[15:8]	VOL_RAMP_RATE_DOWN	Linear step size from current volume to target volume, represented as a fraction of full-scale. $$\text{ramp\_step[dec/sample]} = \frac{\text{VOL\_RAMP\_RATE\_DOWN}^{12}}{2}$$ • 8'h00: Instant change • 8'h01: Slowest change • 8'h20: Default • 8'hFF: Fastest change
[7:0]	VOL_RAMP_RATE_UP	Linear step size from current volume to target volume, represented as a fraction of full-scale. $$\text{ramp\_step[inc/sample]} = \frac{\text{VOL\_RAMP\_RATE\_UP}^{12}}{2}$$ • 8'h00: Instant change • 8'h01: Slowest change • 8'h20: Default • 8'hFF: Fastest change

Register 38: VOLUME RAMP SPEED

Bits	[7:1]	[0]
Default	7'd0	1'b0

Bits	Mnemonic	Description
[7:1]	RESERVED	N/A
[0]	VOL_RAMP_SPEED_SEL	Select the range of ramp rates. • 1'b0: 85ms to 334us (default) • 1'b1: 682ms to 2.70ms

Register 41-39: RESERVED

Register 42: STATUS BITS MASK

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	MASK_DAC_ZCD_CH2	Masks the latched ZERO_CROSS_FLAG status bit on DAC CH2. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[6]	MASK_DAC_ZCD_CH1	Masks the latched ZERO_CROSS_FLAG status bit on DAC CH1. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[5]	MASK_ADC_ZCD_CH2	Masks the latched ZERO_CROSS_FLAG status bit on ADC CH2. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[4]	MASK_ADC_ZCD_CH1	Masks the latched ZERO_CROSS_FLAG status bit on ADC CH1. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[3]	MASK_ADC_OVERLOAD_CH2	Masks the latched ADC_OVERLOAD status bit on ADC CH2. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[2]	MASK_ADC_OVERLOAD_CH1	Masks the latched ADC_OVERLOAD status bit on ADC CH1. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[1]	MASK_PEAK_DET_CH2	Masks the latched PEAK_FLAG status bit on ADC CH2. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[0]	MASK_PEAK_DET_CH1	Masks the latched PEAK_FLAG status bit on ADC CH1. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled

Register 43: STATUS BITS CLEAR

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	CLEAR_DAC_ZCD_CH2	Clears the latched ZERO_CROSS_FLAG status bit on DAC CH2. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[6]	CLEAR_DAC_ZCD_CH1	Clears the latched ZERO_CROSS_FLAG status bit on DAC CH1. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[5]	CLEAR_ADC_ZCD_CH2	Clears the latched ZERO_CROSS_FLAG status bit on ADC CH2. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[4]	CLEAR_ADC_ZCD_CH1	Clears the latched ZERO_CROSS_FLAG status bit on ADC CH1. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[3]	CLEAR_ADC_OVERLOAD_CH2	Clears the latched ADC_OVERLOAD status bit on ADC CH2. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[2]	CLEAR_ADC_OVERLOAD_CH1	Clears the latched ADC_OVERLOAD status bit on ADC CH1. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[1]	CLEAR_PEAK_DET_CH2	Clears the latched PEAK_FLAG status bit on ADC CH2. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[0]	CLEAR_PEAK_DET_CH1	Clears the latched PEAK_FLAG status bit on ADC CH1. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared

Register 60-44: RESERVED

GPIO Registers

Register 61: GPIO1/2 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO2_CFG	Configure GPIO2 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC CH1 Detection flag – output • 4'd8: ADC CH2 Detection flag – output • 4'd9: OR of Status Bits – output • 4'd10: S/PDIF Encoder Stream – output • 4'd11: PWM signal – output • 4'd12: Output 0 – output • 4'd13: ASP Status – Input/Output • 4'd14-15: Reserved
[3:0]	GPIO1_CFG	Configure GPIO1 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC CH1 Detection flag – output • 4'd8: ADC CH2 Detection flag – output • 4'd9: OR of Status Bits – output • 4'd10: S/PDIF Encoder Stream – output • 4'd11: PWM signal – output • 4'd12: Output 0 – output • 4'd13: ASP Status – Input/Output • 4'd14-15: Reserved

Register 62: GPIO3/4 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO4_CFG	Configure GPIO4 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC CH1 Detection flag – output • 4'd8: ADC CH2 Detection flag – output • 4'd9: OR of Status Bits – output • 4'd10: S/PDIF Encoder Stream – output • 4'd11: PWM signal – output • 4'd12: Output 0 – output • 4'd13: ASP Status – Input/Output • 4'd14-15: Reserved
[3:0]	GPIO3_CFG	Configure GPIO3 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC CH1 Detection flag – output • 4'd8: ADC CH2 Detection flag – output • 4'd9: OR of Status Bits – output • 4'd10: S/PDIF Encoder Stream – output • 4'd11: PWM signal – output • 4'd12: Output 0 – output • 4'd13: ASP Status – Input/Output • 4'd14-15: Reserved

Register 63: GPIO5/6 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO6_CFG	Configure GPIO6 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC CH1 Detection flag – output • 4'd8: ADC CH2 Detection flag – output • 4'd9: OR of Status Bits – output • 4'd10: S/PDIF Encoder Stream – output • 4'd11: PWM signal – output • 4'd12: Output 0 – output • 4'd13: ASP Status – Input/Output • 4'd14-15: Reserved
[3:0]	GPIO5_CFG	Configure GPIO5 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC CH1 Detection flag – output • 4'd8: ADC CH2 Detection flag – output • 4'd9: OR of Status Bits – output • 4'd10: S/PDIF Encoder Stream – output • 4'd11: PWM signal – output • 4'd12: Output 0 – output • 4'd13: ASP Status – Input/Output • 4'd14-15: Reserved

Register 64: GPIO7/8 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO8_CFG	Configure GPIO8 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC CH1 Detection flag – output • 4'd8: ADC CH2 Detection flag – output • 4'd9: OR of Status Bits – output • 4'd10: S/PDIF Encoder Stream – output • 4'd11: PWM signal – output • 4'd12: Output 0 – output • 4'd13: ASP Status – Input/Output • 4'd14-15: Reserved
[3:0]	GPIO7_CFG	Configure GPIO7 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC CH1 Detection flag – output • 4'd8: ADC CH2 Detection flag – output • 4'd9: OR of Status Bits – output • 4'd10: S/PDIF Encoder Stream – output • 4'd11: PWM signal – output • 4'd12: Output 0 – output • 4'd13: ASP Status – Input/Output • 4'd14-15: Reserved

Register 65: GPIO9 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3:0]	GPIO9_CFG	Configure GPIO9 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC CH1 Detection flag – output • 4'd8: ADC CH2 Detection flag – output • 4'd9: OR of Status Bits – output • 4'd10: S/PDIF Encoder Stream – output • 4'd11: PWM signal – output • 4'd12: Output 0 – output • 4'd13: ASP Status – Input/Output • 4'd14-15: Reserved

Register 67-66: GPIO INPUT ENABLE

Bits	[15:9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	7'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:9]	RESERVED	N/A
[8]	GPIO9_SDB	• 1'b0: GPIO9 input disabled (default) • 1'b1: GPIO9 input enabled
[7]	GPIO8_SDB	• 1'b0: GPIO8 input disabled (default) • 1'b1: GPIO8 input enabled
[6]	GPIO7_SDB	• 1'b0: GPIO7 input disabled (default) • 1'b1: GPIO7 input enabled
[5]	GPIO6_SDB	• 1'b0: GPIO6 input disabled (default) • 1'b1: GPIO6 input enabled
[4]	GPIO5_SDB	• 1'b0: GPIO5 input disabled (default) • 1'b1: GPIO5 input enabled
[3]	GPIO4_SDB	• 1'b0: GPIO4 input disabled (default) • 1'b1: GPIO4 input enabled
[2]	GPIO3_SDB	• 1'b0: GPIO3 input disabled (default) • 1'b1: GPIO3 input enabled
[1]	GPIO2_SDB	• 1'b0: GPIO2 input disabled (default) • 1'b1: GPIO2 input enabled
[0]	GPIO1_SDB	• 1'b0: GPIO1 input disabled (default) • 1'b1: GPIO1 input enabled

Register 69-68: GPIO OUTPUT ENABLE

Bits	[15:9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	7'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:9]	RESERVED	N/A
[8]	GPIO9_OE	• 1'b0: Tristate GPIO9 output (default) • 1'b1: GPIO9 output enabled
[7]	GPIO8_OE	• 1'b0: Tristate GPIO8 output (default) • 1'b1: GPIO8 output enabled
[6]	GPIO7_OE	• 1'b0: Tristate GPIO7 output (default) • 1'b1: GPIO7 output enabled
[5]	GPIO6_OE	• 1'b0: Tristate GPIO6 output (default) • 1'b1: GPIO6 output enabled
[4]	GPIO5_OE	• 1'b0: Tristate GPIO5 output (default) • 1'b1: GPIO5 output enabled
[3]	GPIO4_OE	• 1'b0: Tristate GPIO4 output (default) • 1'b1: GPIO4 output enabled
[2]	GPIO3_OE	• 1'b0: Tristate GPIO3 output (default) • 1'b1: GPIO3 output enabled
[1]	GPIO2_OE	• 1'b0: Tristate GPIO2 output (default) • 1'b1: GPIO2 output enabled
[0]	GPIO1_OE	• 1'b0: Tristate GPIO1 output (default) • 1'b1: GPIO1 output enabled

Register 71-70: GPIO INVERT

Bits	[15:9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	7'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:9]	RESERVED	N/A
[8]	GPIO9_INV	Invert the GPIO9 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[7]	GPIO8_INV	Invert the GPIO8 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[6]	GPIO7_INV	Invert the GPIO7 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[5]	GPIO6_INV	Invert the GPIO6 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[4]	GPIO5_INV	Invert the GPIO5 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[3]	GPIO4_INV	Invert the GPIO4 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[2]	GPIO3_INV	Invert the GPIO3 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[1]	GPIO2_INV	Invert the GPIO2 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	GPIO1_INV	Invert the GPIO1 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted

Register 73-72: GPIO WEAK KEEPER

Bits	[15:9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	7'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:9]	RESERVED	N/A
[8]	GPIO9_WK_EN	• 1'b0: GPIO9 weak keeper disabled (default) • 1'b1: GPIO9 weak keeper enabled
[7]	GPIO8_WK_EN	• 1'b0: GPIO8 weak keeper disabled (default) • 1'b1: GPIO8 weak keeper enabled
[6]	GPIO7_WK_EN	• 1'b0: GPIO7 weak keeper disabled (default) • 1'b1: GPIO7 weak keeper enabled
[5]	GPIO6_WK_EN	• 1'b0: GPIO6 weak keeper disabled (default) • 1'b1: GPIO6 weak keeper enabled
[4]	GPIO5_WK_EN	• 1'b0: GPIO5 weak keeper disabled (default) • 1'b1: GPIO5 weak keeper enabled
[3]	GPIO4_WK_EN	• 1'b0: GPIO4 weak keeper disabled (default) • 1'b1: GPIO4 weak keeper enabled
[2]	GPIO3_WK_EN	• 1'b0: GPIO3 weak keeper disabled (default) • 1'b1: GPIO3 weak keeper enabled
[1]	GPIO2_WK_EN	• 1'b0: GPIO2 weak keeper disabled (default) • 1'b1: GPIO2 weak keeper enabled
[0]	GPIO1_WK_EN	• 1'b0: GPIO1 weak keeper disabled (default) • 1'b1: GPIO1 weak keeper enabled

Register 75-74: GPIO READ

Bits	[15:9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	7'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:9]	RESERVED	N/A
[8]	GPIO9_READ	• 1'b0: GPIO9 input readback disabled (default) • 1'b1: Allows readback of GPIO9 input
[7]	GPIO8_READ	• 1'b0: GPIO8 input readback disabled (default) • 1'b1: Allows readback of GPIO8 input
[6]	GPIO7_READ	• 1'b0: GPIO7 input readback disabled (default) • 1'b1: Allows readback of GPIO7 input
[5]	GPIO6_READ	• 1'b0: GPIO6 input readback disabled (default) • 1'b1: Allows readback of GPIO6 input
[4]	GPIO5_READ	• 1'b0: GPIO5 input readback disabled (default) • 1'b1: Allows readback of GPIO5 input
[3]	GPIO4_READ	• 1'b0: GPIO4 input readback disabled (default) • 1'b1: Allows readback of GPIO4 input
[2]	GPIO3_READ	• 1'b0: GPIO3 input readback disabled (default) • 1'b1: Allows readback of GPIO3 input
[1]	GPIO2_READ	• 1'b0: GPIO2 input readback disabled (default) • 1'b1: Allows readback of GPIO2 input
[0]	GPIO1_READ	• 1'b0: GPIO1 input readback disabled (default) • 1'b1: Allows readback of GPIO1 input

Register 76: GPIO ADC FLAG CONFIG

Bits	[7:5]	[4]	[3:2]	[1:0]
Default	3'd0	1'b0	2'd0	2'd0

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4]	ADC_LIVE_FLAG_EN	Set the ADC detection flags to use the live value, instead of the latched value. • 1'b0: Latched flags (default) • 1'b1: Live flags
[3:2]	ADC_CH2_DET_FLAG_SEL	Selects which ADC CH2 flag to output when GPIO_CFG is set to "ADC CH1 Detection Flag". • 2'd0: ADC Peak Detect Flag (default) • 2'd1: ADC Overload Flag • 2'd2: ADC Zero-Cross Detect Flag • 2'd3: Reserved
[1:0]	ADC_CH1_DET_FLAG_SEL	Selects which ADC CH1 flag to output when GPIO_CFG is set to "ADC CH1 Detection Flag". • 2'd0: ADC Peak Detect Flag (default) • 2'd1: ADC Overload Flag • 2'd2: ADC Zero-Cross Detect Flag • 2'd3: Reserved

Register 77: GPIO DAC FLAG CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'd0	1'b0	1'b0	1'b0	1'b0	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	DAC_FLAG_CH_SEL	Outputs a specific channel's flag if the corresponding GPIO_AND and GPIO_OR are not set. • 1'b0: Outputs status/flag from CH1 • 1'b1: Outputs status/flag from CH2
[5]	GPIO_OR_SS_RAMP	Sets the GPIO_CFG "Soft Ramp Done" flag output as the bitwise OR of both channel's flags. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is (|ss_full_ramp)
[4]	GPIO_OR_AUTOMUTE	Sets the GPIO_CFG "Automute Status" output as the bitwise OR of both channel's statuses. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is (|automute)
[3]	GPIO_OR_VOL_MIN	Sets the GPIO_CFG "Minimum Volume" flag output as the bitwise OR of both channel's flags. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is (|vol_min)
[2]	GPIO_AND_SS_RAMP	Sets the GPIO_CFG "Soft Ramp Done" flag output as the bitwise AND of both channel's flags. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is (&ss_full_ramp) (default) Note: Overridden by GPIO_OR_SS_RAMP.
[1]	GPIO_AND_AUTOMUTE	Sets the GPIO_CFG "Automute Status" output as the bitwise AND of both channel's statuses. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is (&automute) (default) Note: Overridden by GPIO_OR_AUTOMUTE.
[0]	GPIO_AND_VOL_MIN	Sets the GPIO_CFG "Minimum Volume" flag output as the bitwise AND of both channel's flags. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is (&vol_min) (default) Note: Overridden by GPIO_OR_VOL_MIN.

Register 78: PWM COUNT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	PWM_COUNT	8-bit value for the number of MCLK periods the PWM signal is high. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 80-79: PWM FREQUENCY

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	PWM_FREQ	16-bit value for the frequency of the PWM signal. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $\text{Frequency [Hz]} = \frac{\text{MCLK}}{\text{PWM\_FREQ} + 1}$ $\text{Duty Cycle [\%]} = \left(\frac{\text{PWM\_COUNT}}{\text{PWM\_FREQ} + 1}\right) \cdot 100$

ADC Registers

Register 81: ADC NEGATION

Bits	[7:2]	[1]	[0]
Default	6'b000000	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	ADC_NEG_SEL_CH2	Inverts data input from the CH2 analog ADC. • 1'b0: No inversion (default) • 1'b1: Inverts input data
[0]	ADC_NEG_SEL_CH1	Inverts data input from the CH1 analog ADC. • 1'b0: No inversion (default) • 1'b1: Inverts input data

Register 82: ADC DATAPATH CONTROL

Bits	[7:5]	[4]	[3]	[2:0]
Default	3'd0	1'b0	1'b0	3'b000

Bits	Mnemonic	Description
[7:5]	ADC_FILTER_SHAPE	Selects the 8x decimation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase fast roll-off apodizing • 3'd2: Linear phase fast roll-off • 3'd3: Linear phase fast roll-off low ripple • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion
[4]	ADC_BYPASS_FIR2X	• 1'b0: Non-bypass (default) • 1'b1: Bypass FIR_2x
[3]	ADC_BYPASS_FIR4X	• 1'b0: Non-bypass (default) • 1'b1: Bypass FIR_4x
[2:0]	ADC_BYPASS_IIR	Bypass IIR Filter. • 3'b000: Non-bypass (default) • 3'b111: Bypass IIR

Register 84-83: ADC FILTER CONFIG

Bits	[15:14]	[13]	[12]	[11]	[10]	[9:0]
Default	2'd0	1'b1	1'b1	1'b0	1'b0	10'b1010111111

Bits	Mnemonic	Description
[15:14]	RESERVED	N/A
[13]	DC_BLOCK_EN_CH2	Enable the CH2 DC blocking filter on audio datapath. • 1'b0: Bypass DC blocking filter • 1'b1: Use DC blocking filter (default)
[12]	DC_BLOCK_EN_CH1	Enable the CH1 DC blocking filter on audio datapath. • 1'b0: Bypass DC blocking filter • 1'b1: Use DC blocking filter (default)
[11]	ADC_PROG_FIR_COEFF_WE	Enables writing to the programmable ADC FIR coefficient RAM. • 1'b0: Disables write signal to the coefficient RAM (default) • 1'b1: Enables write signal to the coefficient RAM.
[10]	ADC_PROG_FIR_COEFF_EN	Enables the custom ADC oversampling filter coefficients. • 1'b0: Uses a built-in filter selected by ADC_FILTER_SHAPE (default) • 1'b1: Uses the coefficients programmed via PROG_FIR
[9:0]	RESERVED	N/A

Register 85: ADC PROGRAM FIR ADDRESS

Bits	[7]	[6:0]
Default	1'b0	7'd0

Bits	Mnemonic	Description
[7]	ADC_PROG_FIR_COEFF_STAGE	Selects which stage of the ADC filter to write. • 1'b0: Selects the 2x stage of the oversampling filter (default). • 1'b1: Selects the 4x stage of the oversampling filter.
[6:0]	ADC_PROG_FIR_COEFF_ADDR	Selects the coefficient address when writing custom coefficients for the ADC oversampling filter.

Register 88-86: ADC PROGRAM FIR DATA

Bits	[23:0]
Default	24'd0

Bits	Mnemonic	Description
[23:0]	ADC_PROG_FIR_COEFF_IN	A 24-bit signed filter coefficient to be written to the address defined in ADC_PROG_FIR_COEFF_ADDR.

Register 90-89: ADC VOLUME

Bits	[15:8]	[7:0]
Default	8'h00	8'h00

Bits	Mnemonic	Description
[15:8]	ADC_VOLUME_CH2	CH2 ADC volume. 0dB to -127dB, 0.5dB steps. • 8'h00: 0dB (default) • 8'hFE: -127dB • 8'hFF: Mute
[7:0]	ADC_VOLUME_CH1	CH1 ADC volume. 0dB to -127dB, 0.5dB steps. • 8'h00: 0dB (default) • 8'hFE: -127dB • 8'hFF: Mute

Register 91: ADC DIGITAL GAIN

Bits	[7]	[6:4]	[3]	[2:0]
Default	1'd0	3'd0	1'd0	3'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:4]	ADC_DIGITAL_GAIN_CH2	ADC CH2 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'dn: +(n*6)dB
[3]	RESERVED	N/A
[2:0]	ADC_DIGITAL_GAIN_CH1	ADC CH1 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'dn: +(n*6)dB

Register 92: ADC PHASE INVERSION

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	ADC_VOL_PHASE_INV_CH2	Inverts the phase of VOLUME_CH2. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	ADC_VOL_PHASE_INV_CH1	Inverts the phase of VOLUME_CH1. • 1'b0: Non-inverted (default) • 1'b1: Inverted

Register 96-93: ADC THD COMP

Bits	[31:16]	[15:0]
Default	16'h0000	16'h0000

Bits	Mnemonic	Description
[31:16]	ADC_THD_COMP_C3	A 16-bit signed coefficient for correcting for the ADC 3rd harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$
[15:0]	ADC_THD_COMP_C2	A 16-bit signed coefficient for correcting for the ADC 2nd harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$

Register 97: DETECTOR ENABLES

Bits	[7:6]	[5]	[4]	[3:2]	[1]	[0]
Default	2'd0	1'b0	1'b0	2'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	ADC_ZCD_EN_CH2	Enables the ADC CH2 zero cross detector. • 1'b0: Disabled (default) • 1'b1: Enabled
[4]	ADC_ZCD_EN_CH1	Enables the ADC CH1 zero cross detector. • 1'b0: Disabled (default) • 1'b1: Enabled
[3:2]	RESERVED	N/A
[1]	PEAK_DETECT_EN_CH2	Enables the ADC CH2 peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	PEAK_DETECT_EN_CH1	Enables the ADC CH1 peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 98: PEAK DETECT CONFIG

Bits	[7]	[6]	[5]	[4:0]
Default	1'd0	1'b0	1'b0	5'd10

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	LOCK_PEAK_VALUE	Locks the current peak detector values, for reading back. • 1'b0: Peak detector value can update (default) • 1'b1: Peak detector value locked
[5]	RESERVED	N/A
[4:0]	PEAK_DECAY_RATE	Sets the speed at which the peak detector value will decay when greater than the input signal. • 5'd0: Instant decay • 5'd1: Fastest decay • 5'd10: Default value • 5'd22: Slowest decay • Others: Reserved

Register 100-99: PEAK THRESHOLDS

Bits	[15:8]	[7:0]
Default	8'hFF	8'hFF

Bits	Mnemonic	Description
[15:8]	PEAK_THRESH_CH2	Threshold value to trigger the PEAK_FLAG in the CH2 peak detector. Triggers if the input signal > PEAK_THRESH_CH2. • 8'h01: -48dB • 8'hFF: 0dB (default) $\text{Threshold [dB]} = 20 \cdot \log10\left(\frac{\text{PEAK\_THRESH\_CH2}}{2^8 - 1}\right)$
[7:0]	PEAK_THRESH_CH1	Threshold value to trigger the PEAK_FLAG in the CH1 peak detector. Triggers if the input signal > PEAK_THRESH_CH1. • 8'h01: -48dB • 8'hFF: 0dB (default) $\text{Threshold [dB]} = 20 \cdot \log10\left(\frac{\text{PEAK\_THRESH\_CH1}}{2^8 - 1}\right)$

Register 104-101: RESERVED

DAC Registers

Register 105: DAC FILTER CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2:0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	3'd0

Bits	Mnemonic	Description
[7]	DAC_PROG_FIR_COEFF_WE	Enables writing to the programmable DAC FIR coefficient RAM. • 1'b0: Disables write signal to the coefficient RAM (default) • 1'b1: Enables write signal to the coefficient RAM.
[6]	DAC_PROG_FIR_COEFF_EN	Enables the custom DAC oversampling filter coefficients. • 1'b0: Uses a built-in filter selected by DAC_FILTER_SHAPE (default) • 1'b1: Uses the coefficients programmed via PROG_FIR
[5]	DAC_BYPASS_IIR	Bypass the IIR filter. • 1'b0: Non-bypassed (default) • 1'b1: Bypassed
[4]	DAC_BYPASS_FIR4X	Bypass the 4X FIR filter. • 1'b0: Non-bypassed (default) • 1'b1: Bypassed
[3]	DAC_BYPASS_FIR2X	Bypass the 2X FIR filter. • 1'b0: Non-bypassed (default) • 1'b1: Bypassed
[2:0]	DAC_FILTER_SHAPE	Selects the 8x interpolation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase fast roll-off apodizing • 3'd2: Linear phase fast roll-off • 3'd3: Linear phase fast roll-off low ripple • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion

Register 106: DAC PROGRAM FIR ADDRESS

Bits	[7]	[6:0]
Default	1'b0	7'd0

Bits	Mnemonic	Description
[7]	DAC_PROG_FIR_COEFF_STAGE	Selects which stage of the DAC filter to write. • 1'b0: Selects the 2x stage of the oversampling filter (default). • 1'b1: Selects the 4x stage of the oversampling filter.
[6:0]	DAC_PROG_FIR_COEFF_ADDR	Selects the coefficient address when writing custom coefficients for the DAC oversampling filter.

Register 109-107: DAC PROGRAM FIR DATA

Bits	[23:0]
Default	24'd0

Bits	Mnemonic	Description
[23:0]	DAC_PROG_FIR_COEFF_IN	A 24-bit signed filter coefficient to be written to the address defined in DAC_PROG_FIR_COEFF_ADDR.

Register 111-110: DAC VOLUME

Bits	[15:8]	[7:0]
Default	8'h02	8'h02

Bits	Mnemonic	Description
[15:8]	DAC_VOLUME_CH2	DAC CH2 volume. +1dB to -126dB, 0.5dB steps • 8'h00: +1dB • 8'h02: 0dB (default) • 8'hFE: -126dB • 8'hFF: Mute
[7:0]	DAC_VOLUME_CH1	DAC CH1 volume. +1dB to -126dB, 0.5dB steps • 8'h00: +1dB • 8'h02: 0dB (default) • 8'hFE: -126dB • 8'hFF: Mute

Register 113-112: DIRECT MONITOR VOLUME

Bits	[15:8]	[7:0]
Default	8'hFF	8'hFF

Bits	Mnemonic	Description
[15:8]	DIR_MON_VOL_CH2	Volume of ADC CH2 direct monitor signal added into DAC CH2. +1dB to -126dB, 0.5dB steps. • 8'h00: +1dB • 8'h02: 0dB • 8'hFE: -126dB • 8'hFF: -inf dB (default)
[7:0]	DIR_MON_VOL_CH1	Volume of ADC CH1 direct monitor signal added into DAC CH1. +1dB to -126dB, 0.5dB steps. • 8'h00: +1dB • 8'h02: 0dB • 8'hFE: -126dB • 8'hFF: -inf dB (default)

Register 114: DAC DIGITAL GAIN

Bits	[7]	[6:4]	[3]	[2:0]
Default	1'd0	3'd0	1'd0	3'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:4]	DAC_DIGITAL_GAIN_CH2	DAC CH2 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'dn: +(n*6)dB
[3]	RESERVED	N/A
[2:0]	DAC_DIGITAL_GAIN_CH1	DAC CH1 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'dn: +(n*6)dB

Register 115: DAC PHASE INVERSION

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DAC_ZCD_EN_CH2	Enables the DAC CH2 zero cross detector. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	DAC_ZCD_EN_CH1	Enables the DAC CH1 zero cross detector. • 1'b0: Disabled (default) • 1'b1: Enabled
[5]	DIR_MON_MONO_CH2	Adds both ADC direct monitor signals onto the CH2 DAC datapath. Both signals are controlled by the CH2 volume and mute controls. • 1'b0: Disabled, CH2 ADC monitored on CH2 DAC (default) • 1'b1: Enabled, CH1 ADC & CH2 ADC monitored on CH2 DAC
[4]	DIR_MON_MONO_CH1	Adds both ADC direct monitor signals onto the CH1 DAC datapath. Both signals are controlled by the CH1 volume and mute controls. • 1'b0: Disabled, CH1 ADC monitored on CH1 DAC (default) • 1'b1: Enabled, CH1 ADC & CH2 ADC monitored on CH1 DAC
[3]	DIR_MON_VOL_PHASE_INV_CH2	Inverts the phase of DIR_MON_VOL_CH2. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[2]	DIR_MON_VOL_PHASE_INV_CH1	Inverts the phase of DIR_MON_VOL_CH1. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[1]	DAC_VOL_PHASE_INV_CH2	Inverts the phase of DAC_VOLUME_CH2. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	DAC_VOL_PHASE_INV_CH1	Inverts the phase of DAC_VOLUME_CH1. • 1'b0: Non-inverted (default) • 1'b1: Inverted

Register 116: DAC MUTE

Bits	[7:6]	[5]	[4]	[3:2]	[1]	[0]
Default	2'd0	1'b0	1'b0	2'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	DIR_MON_MUTE_CH2	Mutes the CH2 ADC direct monitor signal. • 1'b0: Normal operation (default) • 1'b1: Direct monitor signal muted
[4]	DIR_MON_MUTE_CH1	Mutes the CH1 ADC direct monitor signal. • 1'b0: Normal operation (default) • 1'b1: Direct monitor signal muted
[3:2]	RESERVED	N/A
[1]	DAC_MUTE_CH2	Mutes the CH2 DAC datapath, will not mute the monitor signal. • 1'b0: Normal CH2 operation (default) • 1'b1: Mute CH2 DAC
[0]	DAC_MUTE_CH1	Mutes the CH1 DAC datapath, will not mute the monitor signal. • 1'b0: Normal CH1 operation (default) • 1'b1: Mute CH1 DAC

Register 117: SOFT RAMP CONFIG

Bits	[7]	[6]	[5]	[4]	[3:0]
Default	1'b0	1'b0	1'b1	1'd0	4'd3

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	DIR_MON_ADC_SEL	Selects the Direct Monitor source, from the ADC datapath. • 1'b0: Pre-ASP, minimizes delay (default) • 1'b1: Post-ASP
[5]	MUTE_RAMP_TO_GROUND	• 1'b0: When ramped to min volume during normal mute, do not soft ramp to ground • 1'b1: When ramped to min volume during normal mute, soft ramp to ground for power saving (default) normal mute includes: automute, mute by register, mute by GPIO
[4]	RESERVED	N/A
[3:0]	SOFT_RAMP_TIME	Sets the amount of time that it takes to perform a soft start ramp. This time affects both ramp to ground and ramp to AVCC/2. Valid from 0 to 15 (inclusive) $\text{Time [s]} = \frac{2^{16} \cdot 2^{\text{SOFT\_RAMP\_TIME}}}{MCLK \cdot 2^{\sim\text{MCLK\_24M\_DIV2}}}$

Register 119-118: DC OFFSET

Bits	[15:8]	[7:0]
Default	8'h00	8'h00

Bits	Mnemonic	Description
[15:8]	DC_OFFSET_CH2	Signed 8-bit DC offset value added to the CH2 datapath signal, 100 uV/step. • 8'hFF: -12.8mV DC Offset • 8'h00: 0mV DC Offset (default) • 8'h7F: 12.7mV DC Offset
[7:0]	DC_OFFSET_CH1	Signed 8-bit DC offset value added to the CH1 datapath signal, 100 uV/step. • 8'hFF: -12.8mV DC Offset • 8'h00: 0mV DC Offset (default) • 8'h7F: 12.7mV DC Offset

Register 120: AUTOMUTE ENABLE

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b1	1'b1

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	AUTOMUTE_EN_CH2	Enables CH2 automute. • 1'b0: Disabled • 1'b1: Enabled (default)
[0]	AUTOMUTE_EN_CH1	Enables CH1 automute. • 1'b0: Disabled • 1'b1: Enabled (default)

Register 122-121: AUTOMUTE CONFIG

Bits	[15]	[14]	[13]	[12:11]	[10:0]
Default	1'b1	1'b1	1'b1	2'd0	11'h0F

Bits	Mnemonic	Description
[15]	DSD_FAULT_DET_EN	Enables the DSD fault detection logic. • 1'b0: Disabled • 1'b1: Enabled (default)
[14]	DSD_DC_AM_EN	Enables the DSD automute condition, if a DC level is detected. • 1'b0: Disabled • 1'b1: Enabled (default)
[13]	DSD_MUTE_AM_EN	Enables the DSD automute condition, if a DSD mute pattern is detected. • 1'b0: Disabled • 1'b1: Enabled (default)
[12:11]	RESERVED	N/A
[10:0]	AUTOMUTE_TIME	Configures the amount of time in seconds the audio must remain below AUTOMUTE_LEVEL before an automute condition is flagged. • 11'h000: Disabled • 11'h001: Slowest • 11'h00F: Default • 11'h7FF: Fastest $\text{Time [s]} = \frac{2^{18}}{\text{AUTOMUTE\_TIME} \cdot FS}$

Register 126-123: AUTOMUTE LEVEL

Bits	[31:16]	[15:0]
Default	16'h000A	16'h0008

Bits	Mnemonic	Description
[31:16]	AUTOMUTE_OFF_LEVEL	The threshold which the audio must be above before the automute condition is immediately cleared. • 16'h0001: -138dB • 16'h000A: -118dB (default) • 16'hFFFF: -42dB $\text{level [dB]} = 20 \cdot \log10\left(\frac{\text{AUTOMUTE\_OFF\_LEVEL}}{(2^{16}-1)\cdot 2^{7}}\right)$
[15:0]	AUTOMUTE_LEVEL	The threshold which the audio must be below before an automute condition is flagged. • 16'h0001: -138dB • 16'h0008: -120dB (default) • 16'hFFFF: -42dB $\text{level [dB]} = 20 \cdot \log10\left(\frac{\text{AUTOMUTE\_LEVEL}}{(2^{16}-1)\cdot 2^{7}}\right)$

Register 130-127: DAC THD COMP

Bits	[31:28]	[27:16]	[15:12]	[11:0]
Default	4'd0	12'h000	4'd0	12'h000

Bits	Mnemonic	Description
[31:28]	RESERVED	N/A
[27:16]	DAC_THD_COMP_C3	A 12-bit signed coefficient for correcting for the DAC 3rd harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$
[15:12]	RESERVED	N/A
[11:0]	DAC_THD_COMP_C2	A 12-bit signed coefficient for correcting for the DAC 2nd harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$

Register 135-131: RESERVED

PLL Registers

Register 136: PLL CLOCK SELECT

Bits	[7]	[6]	[5:4]	[3]	[2]	[1:0]
Default	1'b0	1'b0	2'b10	1'b0	1'b0	2'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	PLL_CLK_PHASE_INV	Inverts the PLL output clock. • 1'b0: Uninverted (default) • 1'b1: Inverted
[5:4]	SEL_PLL_CLK_IN	Selects PLL input clock source when EN_PLL_CLK_IN is set. • 2'b00: ACLK1 • 2'b01: ACLK2 • 2'b10: DCLK (default) • 2'b11: CLK_UPSMP
[3]	EN_PLL_CLK_IN	Allows SEL_PLL_CLK_IN to select PLL input clocks. • 1'b0: Disables SEL_PLL_CLK_IN (default) • 1'b1: Enables SEL_PLL_CLK_IN
[2]	SEL_MCLK_IN_PLL	Selects which ACLK source is used by the digital core and analog ADC, when EN_MCLK_IN is set. • 1'b0: ACLK1/2 (default) • 1'b1: PLL_CLK Note: Overrides SEL_MCLK_ACLK_SRC.
[1:0]	RESERVED	N/A

Register 137: PLL VCO & CP

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	4'b0100	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	PLL_CP_EN	Enables/disables the PLL charge pump. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	PLL_VCO_EN	Enables/disables the PLL voltage-controlled oscillator (VCO). • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	PLL_CLKSMP_EN	Power Down the PLL circuitry. • 1'b0: PLL Block disabled (default) • 1'b1: PLL Block enabled
[0]	PLL_DIG_RSTB	Enable the Digital Core of the PLL. • 1'b0: PLL Digital Core disabled (default) • 1'b1: PLL Digital Core enabled

Register 138: PLL REGULATOR

Bits	[7]	[6:2]	[1]	[0]
Default	1'b1	5'b00000	1'b1	1'b0

Bits	Mnemonic	Description
[7]	PLL_FB_DIV_LOAD	Write 1'b1 then write 1'b0 to load CLK_FB_DIV.
[6:2]	RESERVED	N/A
[1]	PLL_REG_LN	Select low noise reference for PLL regulator. • 1'b0: Disabled (default) • 1'b1: Enabled Note: Requires low noise analog reference voltage. Turns on <AREF_LN_DLY>ms after AREF_EN.
[0]	PLL_REG_EN	Enable the PLL regulator. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 141-139: PLL FEEDBACK DIV

Bits	[23:0]
Default	24'h100000

Bits	Mnemonic	Description
[23:0]	PLL_CLK_FB_DIV	Sets the PLL clock feedback divider (Nfb). • 24'hn: Divide by 2^25/n

Register 143-142: PLL IN & OUT DIV

Bits	[15:13]	[12]	[11:8]	[7:4]	[3:0]
Default	3'd0	1'b1	4'd0	4'd3	4'd0

Bits	Mnemonic	Description
[15:13]	RESERVED	N/A
[12]	PLL_CLK_OUT_DIV_PHASE_EN	Sets the tuning mode for the PLL_CLK_OUT_DIV phase. • 1'b0: Dynamic Tuning of Phase (recommended for ASYNC PLL case) • 1'b1: Static Tuning of Phase (default)
[11:8]	RESERVED	N/A
[7:4]	PLL_CLK_OUT_DIV	Sets the PLL clock output divider (No). • 4'dn: Divide by (n + 1).
[3:0]	PLL_CLK_IN_DIV	Sets the PLL clock input divider (Ni). • 4'dn: Divide by (n + 1).

Register 146-144: RESERVED

ASP Registers

Register 147: ASP CONTROL

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b1	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ASP_DAC_CORE_EN	Enables programmed DAC ASP functionality. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	ASP_DAC_MEM_FLUSH	Flushes the DAC ASP memories, clearing any existing programming. Requires ASP_DAC_CORE_EN to not be set.
[5]	ASP_SPI_FLASH_REG_RUN	Toggle to transfer a byte of data from the I2C registers over the SPI master interface.
[4]	RESERVED	N/A
[3]	ASP_PROG_SOURCE_SEL	Selects which interface programs the ASP. • 1'b0: I2C programming (default) • 1'b1: SPI master programming
[2]	ASP_ADC_MEM_FLUSH	Flushes the ADC ASP memories, clearing any existing programming. Requires ASP_ADC_CORE_EN to not be set.
[1]	ASP_PROG_EN	Enables ASP programming. Programmed functionality overridden. • 1'b0: Programming disabled (default) • 1'b1: Programming enabled
[0]	ASP_ADC_CORE_EN	Enables programmed ASP functionality. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 148: ASP BYPASS

Bits	[7:6]	[5]	[4]	[3:2]	[1]	[0]
Default	2'd0	1'b0	1'b0	2'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	ASP_DAC_BYPASS_CH2	Bypasses the DAC ASP core, but leaves it running. • 1'b0: Un-bypassed (default) • 1'b1: Bypassed
[4]	ASP_DAC_BYPASS_CH1	Bypasses the DAC ASP core, but leaves it running. • 1'b0: Un-bypassed (default) • 1'b1: Bypassed
[3:2]	RESERVED	N/A
[1]	ASP_ADC_BYPASS_CH2	Bypasses the ADC ASP core, but leaves it running. • 1'b0: Un-bypassed (default) • 1'b1: Bypassed
[0]	ASP_ADC_BYPASS_CH1	Bypasses the ADC ASP core, but leaves it running. • 1'b0: Un-bypassed (default) • 1'b1: Bypassed

Register 149: RESERVED

Register 150: ASP PAIRED MODE

Bits	[7:6]	[5]	[4]	[3:2]	[1:0]
Default	2'd0	1'b0	1'b0	2'd0	2'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	ASP_DAC_PAIRED_MODE	Enables the DAC ASP core paired mode. • 1'b0: Disabled (default) • 1'b1: Enabled
[4]	ASP_ADC_PAIRED_MODE	Enables the ADC ASP core paired mode. • 1'b0: Disabled (default) • 1'b1: Enabled
[3:2]	RESERVED	N/A
[1:0]	ASP_CORE_READ_SEL	Determines the ASP core connected to the readback registers. • 2'd0: ADC CH1 (default) • 2'd1: ADC CH2 • 2'd2: DAC CH1 • 2'd3: DAC CH2

Register 151: ASP INPUT3 SELECT

Bits	[7:6]	[5]	[4]	[3:2]	[1]	[0]
Default	2'd0	1'b0	1'b0	2'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	ASP_DAC_IN3_SEL_CH2	Selects DAC CH2 ASP core input3 connection. • 1'b0: ADC CH2 data (default) • 1'b1: GPIO Input flags
[4]	ASP_DAC_IN3_SEL_CH1	Selects DAC CH1 ASP core input3 connection. • 1'b0: ADC CH1 data (default) • 1'b1: GPIO Input flags
[3:2]	RESERVED	N/A
[1]	ASP_ADC_IN3_SEL_CH2	Selects ADC CH2 ASP core input3 connection. • 1'b0: DAC CH2 data (default) • 1'b1: GPIO Input flags
[0]	ASP_ADC_IN3_SEL_CH1	Selects ADC CH1 ASP core input3 connection. • 1'b0: DAC CH1 data (default) • 1'b1: GPIO Input flags

Register 152: ASP PRAM WRITE EN

Bits	[7]	[6]	[5:2]	[1]	[0]
Default	1'b0	1'b0	4'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ASP_DAC_IN3_MIX_SEL	Selects the data point for the DAC ASP core input3 connection. • 1'b0: Pre-ASP ADC datapath (default) • 1'b1: Post-ASP ADC datapath
[6]	ASP_ADC_IN3_MIX_SEL	Selects the data point for the ADC ASP core input3 connection. • 1'b0: Pre-ASP DAC datapath (default) • 1'b1: Post-ASP DAC datapath
[5:2]	RESERVED	N/A
[1]	ASP_DAC_PRAM_WE	Enables writing to the DAC ASP's program (PRAM) memory. Memory shared between all DAC ASP cores. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ASP_ADC_PRAM_WE	Enables writing to the ADC ASP's program (PRAM) memory. Memory shared between all ADC ASP cores. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 153: ASP COEFF DATA WRITE EN

Bits	[7:6]	[5]	[4]	[3:2]	[1]	[0]
Default	2'd0	1'b0	1'b0	2'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	ASP_DAC_COEFF_DATA_WE_CH2	Enables writing to the DAC CH2 ASP core's coefficient (CRAM) and data (DRAM) memories. • 1'b0: Disabled (default) • 1'b1: Enabled
[4]	ASP_DAC_COEFF_DATA_WE_CH1	Enables writing to the DAC CH1 ASP core's coefficient (CRAM) and data (DRAM) memories. • 1'b0: Disabled (default) • 1'b1: Enabled
[3:2]	RESERVED	N/A
[1]	ASP_ADC_COEFF_DATA_WE_CH2	Enables writing to the ADC CH2 ASP core's coefficient (CRAM) and data (DRAM) memories. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ASP_ADC_COEFF_DATA_WE_CH1	Enables writing to the ADC CH1 ASP core's coefficient (CRAM) and data (DRAM) memories. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 154: ASP PROG MEM ADDR

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	ASP_PROG_MEM_ADDR	Selects the address of the programmable memories when programming the ASP. If writing to the CRAM or DRAM ASP_PROG_MEM_ADDR[7] selects the momory accessed. • 1'b0: DRAM • 1'b1: CRAM When ASP programming is disabled, acts as the DMA_ADDR offset.

Register 158-155: ASP PROG MEM DATA

Bits	[31:0]
Default	32'd0

Bits	Mnemonic	Description
[31:0]	ASP_PROG_MEM_DATA	32-bit data written to the programmable memories at address ASP_PROG_MEM_ADDR. The memory written depends on which write enable is toggled. If writing to PRAM, use ASP_PROG_RAM_WE, and the data format is {insn[i + 256], insn[i]}. If writing to CRAM or DRAM, use ASP_COEFF_DATA_WE_CHx. When ASP programming is disabled, control acts as the DMA_DATA1 element.

Register 162-159: DMA DATA2

Bits	[31:0]
Default	32'd0

Bits	Mnemonic	Description
[31:0]	DMA_DATA2	32-bit coefficient stack data written to the ASP core coeff stack at address ASP_DMA_ADDR + 1.

Register 166-163: DMA DATA3

Bits	[31:0]
Default	32'd0

Bits	Mnemonic	Description
[31:0]	DMA_DATA3	32-bit coefficient stack data written to the ASP core coeff stack at address ASP_DMA_ADDR + 2.

Register 170-167: DMA DATA4

Bits	[31:0]
Default	32'd0

Bits	Mnemonic	Description
[31:0]	DMA_DATA4	32-bit coefficient stack data written to the ASP core coeff stack at address ASP_DMA_ADDR + 3.

Register 174-171: DMA DATA5

Bits	[31:0]
Default	32'd0

Bits	Mnemonic	Description
[31:0]	DMA_DATA5	32-bit coefficient stack data written to the ASP core coeff stack at address ASP_DMA_ADDR + 4.

Register 178-175: DMA DATA6

Bits	[31:0]
Default	32'd0

Bits	Mnemonic	Description
[31:0]	DMA_DATA6	32-bit coefficient stack data written to the ASP core coeff stack at address ASP_DMA_ADDR + 5.

Register 182-179: DMA DATA7

Bits	[31:0]
Default	32'd0

Bits	Mnemonic	Description
[31:0]	DMA_DATA7	32-bit coefficient stack data written to the ASP core coeff stack at address ASP_DMA_ADDR + 6.

Register 186-183: DMA DATA8

Bits	[31:0]
Default	32'd0

Bits	Mnemonic	Description
[31:0]	DMA_DATA8	32-bit coefficient stack data written to the ASP core coeff stack at address ASP_DMA_ADDR + 7.

Register 187: DMA CORE MASK

Bits	[7:6]	[5]	[4]	[3:2]	[1]	[0]
Default	2'd0	1'b0	1'b0	2'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	DMA_DAC_CORE_MASK_CH2	Masks the DAC CH2 ASP core, allowing it to update the core's coeff stack with the DMA values. • 1'b0: Disabled (default) • 1'b1: Enabled
[4]	DMA_DAC_CORE_MASK_CH1	Masks the DAC CH1 ASP core, allowing it to update the core's coeff stack with the DMA values. • 1'b0: Disabled (default) • 1'b1: Enabled
[3:2]	RESERVED	N/A
[1]	DMA_ADC_CORE_MASK_CH2	Masks the ADC CH2 ASP core, allowing it to update the core's coeff stack with the DMA values. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	DMA_ADC_CORE_MASK_CH1	Masks the ADC CH1 ASP core, allowing it to update the core's coeff stack with the DMA values. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 188: DMA WRITE EN

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DMA_DATA8_WE	DMA DATA8 write enable, loads into CRAM[DMA_ADDR+7]. Toggle to 1'b0 before updating DMA_DATA8 or DMA_ADDR. • 1'b0: DMA load inactive (default) • 1'b1: DMA load active
[6]	DMA_DATA7_WE	DMA DATA7 write enable, loads into CRAM[DMA_ADDR+6]. Toggle to 1'b0 before updating DMA_DATA7 or DMA_ADDR. • 1'b0: DMA load inactive (default) • 1'b1: DMA load active
[5]	DMA_DATA6_WE	DMA DATA6 write enable, loads into CRAM[DMA_ADDR+5]. Toggle to 1'b0 before updating DMA_DATA6 or DMA_ADDR. • 1'b0: DMA load inactive (default) • 1'b1: DMA load active
[4]	DMA_DATA5_WE	DMA DATA5 write enable, loads into CRAM[DMA_ADDR+4]. Toggle to 1'b0 before updating DMA_DATA5 or DMA_ADDR. • 1'b0: DMA load inactive (default) • 1'b1: DMA load active
[3]	DMA_DATA4_WE	DMA DATA4 write enable, loads into CRAM[DMA_ADDR+3]. Toggle to 1'b0 before updating DMA_DATA4 or DMA_ADDR. • 1'b0: DMA load inactive (default) • 1'b1: DMA load active
[2]	DMA_DATA3_WE	DMA DATA3 write enable, loads into CRAM[DMA_ADDR+2]. Toggle to 1'b0 before updating DMA_DATA3 or DMA_ADDR. • 1'b0: DMA load inactive (default) • 1'b1: DMA load active
[1]	DMA_DATA2_WE	DMA DATA2 write enable, loads into CRAM[DMA_ADDR+1]. Toggle to 1'b0 before updating DMA_DATA2 or DMA_ADDR. • 1'b0: DMA load inactive (default) • 1'b1: DMA load active
[0]	DMA_DATA1_WE	DMA DATA1 write enable, loads into CRAM[DMA_ADDR]. Toggle to 1'b0 before updating DMA_DATA1 or DMA_ADDR. • 1'b0: DMA load inactive (default) • 1'b1: DMA load active

Register 197-189: RESERVED

Register 198: SPI MASTER CONFIG

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	4'd0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:4]	SPI_M_PULSE_WIDTH	Sets the master SCLK frequency. $SCLK[Hz] = \frac{\text{MCLK}}{2 \cdot SPI\_M\_PULSE\_WIDTH}$
[3]	SPI_M_EN	Enable the SPI Master • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	SPI_M_MODE	SPI Mode • 1'b0: Mode 0 (default) • 1'b1: Mode 3
[1]	SPI_M_SEND_BYTE	Triggers the SPI master to send the current byte in SPI_M_DATA_O to the slave device. • 1'b0: Do not send byte (default) • 1'b1: Send byte to SPI slave device
[0]	SPI_M_START	Start/stop SPI master transactions. • 1'b0: Transactions stopped (default) • 1'b1: Transactions started

Register 199: SPI MASTER DATA OUT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	SPI_M_DATA_O	Data byte to send over the SPI master interface.

Readback Registers

Register 218: OUTPUT FMT VALIDITY READ

Bits	[7:4]	[3:1]	[0]
Default	-	-	-

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3:1]	OUTPUT_DATA_FORMAT_SEL_OVR	Readback of the current output data format. Either the manual value, or the result of OUTPUT_FMT_FLW_INPUT if enabled. • 3'd0: PCM • 3'd1: DoP • 3'd2: DSD • 3'd3: PDM • 3'd4: S/PDIF • 3'd5: DoPoS
[0]	TDM_ENC_VALID	TDM encoder valid flag.

Register 219: INPUT FMT VALIDITY READ

Bits	[7]	[6:4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	PLL_LOCKED	PLL locked flag.
[6:4]	INPUT_DATA_FORMAT_SEL_OVR	Readback of the current input data format. Either the manual value, or the result of AUTO_DATA_FORMAT_SEL if enabled. • 3'd0: PCM • 3'd1: DoP • 3'd2: DSD • 3'd3: PDM • 3'd4: S/PDIF • 3'd5: DoPoS
[3]	UPSMP_LOCK	CLK Upsampler locked flag.
[2]	SPDIF_DEC_VALID	S/PDIF decoder valid flag.
[1]	DOP_DEC_VALID	DoP decoder valid flag.
[0]	TDM_DEC_VALID	TDM decoder valid flag.

Register 220: AUTO FS READ

Bits	[7]	[6]	[5:0]
Default	-	-	-

Bits	Mnemonic	Description
[7]	EN_64FS_MODE_AUTO	Result {Z} of the automatic sample rate detect (reg0[3] AUTO_FS_DETECT) logic, running the device in 64FS mode. • 1'b0: 64FS disabled • 1'b1: 64FS enabled
[6]	MCLK_128FS_HALF_DIV_AUTO	Result {Y} of the automatic sample rate detect (reg0[3] AUTO_FS_DETECT) logic. • 1'b0: MCLK_128FS is an integer multiple of MCLK, Y = 1. • 1'b1: MCLK_128FS is a (X+1)*0.5 multiple of MCLK, Y = 2.
[5:0]	MCLK_128FS_DIV_AUTO	Result {X} of the automatic sample rate detect (reg0[3] AUTO_FS_DETECT) logic. $FS[Hz] = \frac{Y \cdot MCLK}{(X+1) \cdot \left(\frac{128^Z}{2}\right)}$

Register 221: CLOCK VALIDITY

Bits	[7]	[6]	[5]	[4:0]
Default	-	-	-	-

Bits	Mnemonic	Description
[7]	RATIO_VALID	Validity of the MCLK/MCLK_128FS ratio. • 1'b0: Invalid ratio • 1'b1: Valid ratio
[6]	BCK_INVALID	Validity of the BCK signal, requires BCK_MONITOR to be enabled.
[5]	WS_INVALID	Validity of the WS signal, requires WS_MONITOR to be enabled.
[4:0]	AUTO_CH_NUM	Automatic TDM channel number tuning result.

Register 222: S/PDIF DATA READ

Bits	[7:0]
Default	-

Bits	Mnemonic	Description
[7:0]	SPDIF_DEC_DATA_READ	Contains 1 byte of the S/PDIF decoder payload. Byte is controlled by Register 25[4:0] SPDIF_DEC_PAYLOAD_SEL.

Register 224-223: RESERVED

Register 225: CHIP ID

Bits	[7:0]
Default	8'hAF

Bits	Mnemonic	Description
[7:0]	CHIP_ID	• ES9292QPRO: 0xAF

Register 229-226: RESERVED

Register 231-230: GPIO READBACK

Bits	[15:9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[15:9]	RESERVED	N/A
[8]	GPIO9_R	GPIO9 input readback.
[7]	GPIO8_R	GPIO8 input readback.
[6]	GPIO7_R	GPIO7 input readback.
[5]	GPIO6_R	GPIO6 input readback.
[4]	GPIO5_R	GPIO5 input readback.
[3]	GPIO4_R	GPIO4 input readback.
[2]	GPIO3_R	GPIO3 input readback.
[1]	GPIO2_R	GPIO2 input readback.
[0]	GPIO1_R	GPIO1 input readback.

Register 232: ADC CLIP DETECT FLAGS

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	ADC_OVERLOAD_FLAG_LAT_CH2	Latched CH2 ADC modulator overload flag. • 1'b0: No overload • 1'b1: ADC modulator overloaded Note: Requires Reg43[3] CLEAR_CH2_ADC_OVERLOAD to clear flag.
[6]	ADC_OVERLOAD_FLAG_LAT_CH1	Latched CH1 ADC modulator overload flag. • 1'b0: No overload • 1'b1: ADC modulator overloaded Note: Requires Reg43[2] CLEAR_CH1_ADC_OVERLOAD to clear flag.
[5]	ADC_OVERLOAD_FLAG_CH2	CH2 ADC modulator overload flag. • 1'b0: No overload • 1'b1: ADC modulator overloaded
[4]	ADC_OVERLOAD_FLAG_CH1	CH1 ADC modulator overload flag. • 1'b0: No overload • 1'b1: ADC modulator overloaded
[3]	PEAK_FLAG_LAT_CH2	ADC CH2 latched peak detector flag. • 1'b0: CH2 input signal ≤ PEAK_THRESH_CH2 • 1'b1: CH2 input signal > PEAK_THRESH_CH2 Note: Requires Reg43[1] CLEAR_CH2_PEAK_DET to clear flag.
[2]	PEAK_FLAG_LAT_CH1	ADC CH1 latched peak detector flag. • 1'b0: CH1 input signal ≤ PEAK_THRESH_CH1 • 1'b1: CH1 input signal > PEAK_THRESH_CH1 Note: Requires Reg43[0] CLEAR_CH1_PEAK_DET to clear flag.
[1]	PEAK_FLAG_CH2	ADC CH2 peak detector flag. • 1'b0: CH2 input signal ≤ PEAK_THRESH_CH2 • 1'b1: CH2 input signal > PEAK_THRESH_CH2
[0]	PEAK_FLAG_CH1	ADC CH1 peak detector flag. • 1'b0: CH1 input signal ≤ PEAK_THRESH_CH1 • 1'b1: CH1 input signal > PEAK_THRESH_CH1

Register 233: ADC ZERO CROSS FLAGS

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	ADC_ZERO_CROSS_LAT_CH2	ADC CH2 latched zero cross detection flag. Note: Requires Reg43[5] CLEAR_CH2_ZERO_CROSS_DET to clear flag.
[2]	ADC_ZERO_CROSS_LAT_CH1	ADC CH1 latched zero cross detection flag. Note: Requires Reg43[4] CLEAR_CH1_ZERO_CROSS_DET to clear flag.
[1]	ADC_ZERO_CROSS_CH2	ADC CH2 live zero cross detection flag.
[0]	ADC_ZERO_CROSS_CH1	ADC CH1 live zero cross detection flag.

Register 237-234: PEAK READ

Bits	[31:16]	[15:0]
Default	-	-

Bits	Mnemonic	Description
[31:16]	PEAK_LEVEL_CH2	ADC CH2 peak detector value readback. $\text{Peak [dB]} = 20 \cdot \log10\left(\frac{\text{PEAK\_LEVEL\_CH2}}{2^{16}-1}\right)$
[15:0]	PEAK_LEVEL_CH1	ADC CH1 peak detector value readback. $\text{Peak [dB]} = 20 \cdot \log10\left(\frac{\text{PEAK\_LEVEL\_CH1}}{2^{16}-1}\right)$

Register 240-238: ADC PROG FIR COEFF OUT READ

Bits	[23:0]
Default	-

Bits	Mnemonic	Description
[23:0]	PROG_FIR_COEFF_OUT_ADC	Programmable FIR coefficient readback for the ADC.

Register 241: DAC LIVE STATUS FLAGS

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	SS_RAMP_DOWN_CH2	CH2 soft ramped down flag.
[6]	SS_RAMP_DOWN_CH1	CH1 soft ramped down flag.
[5]	SS_RAMP_UP_CH2	CH2 soft ramped up flag.
[4]	SS_RAMP_UP_CH1	CH1 soft ramped up flag.
[3]	AUTOMUTE_CH2	CH2 automute status flag.
[2]	AUTOMUTE_CH1	CH1 automute status flag.
[1]	VOL_MIN_CH2	CH2 minimum volume flag.
[0]	VOL_MIN_CH1	CH1 minimum volume flag.

Register 242: DAC ZERO CROSS FLAGS

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	DAC_ZERO_CROSS_LAT_CH2	DAC CH2 latched zero cross detection flag. Note: Requires Reg43[7] CLEAR_CH2_ZERO_CROSS_DET to clear flag.
[2]	DAC_ZERO_CROSS_LAT_CH1	DAC CH1 latched zero cross detection flag. Note: Requires Reg43[6] CLEAR_CH1_ZERO_CROSS_DET to clear flag.
[1]	DAC_ZERO_CROSS_CH2	DAC CH2 live zero cross detection flag.
[0]	DAC_ZERO_CROSS_CH1	DAC CH1 live zero cross detection flag.

Register 245-243: DAC PROG FIR COEFF OUT READ

Bits	[23:0]
Default	-

Bits	Mnemonic	Description
[23:0]	PROG_FIR_COEFF_OUT_DAC	Programmable FIR coefficient readback for the DAC.

Register 246: RESERVED

Register 248-247: SPI MASTER BUSY

Bits	[15]	[14:13]	[12]	[11:0]
Default	-	-	-	-

Bits	Mnemonic	Description
[15]	SPI_M_ASP_PROG_BUSY	State of the SPI master bus, during the automated ASP programming. • 1'b0: SPI master bus idle • 1'b1: SPI master bus busy
[14:13]	RESERVED	N/A
[12]	SPI_M_FULL_BYTE	Flag indicating the SPI master has complete a full byte of data transfer.
[11:0]	RESERVED	N/A

Register 250-249: RESERVED

Register 253-251: ASP CORE OUTPUT2

Bits	[23:0]
Default	-

Bits	Mnemonic	Description
[23:0]	ASP_OUT2_READ	Signed readback of an ASP core output2 value. Channel output determined by Reg139[6:4] ASP2_CORE_READ_SEL.

Register 254: RESERVED

Register 255: SPI MASTER DATA IN

Bits	[7:0]
Default	-

Bits	Mnemonic	Description
[7:0]	SPI_M_DATA_I	Byte of data read from the SPI slave device.

ES9292PRO Reference Schematic

Hardware (HW) Mode

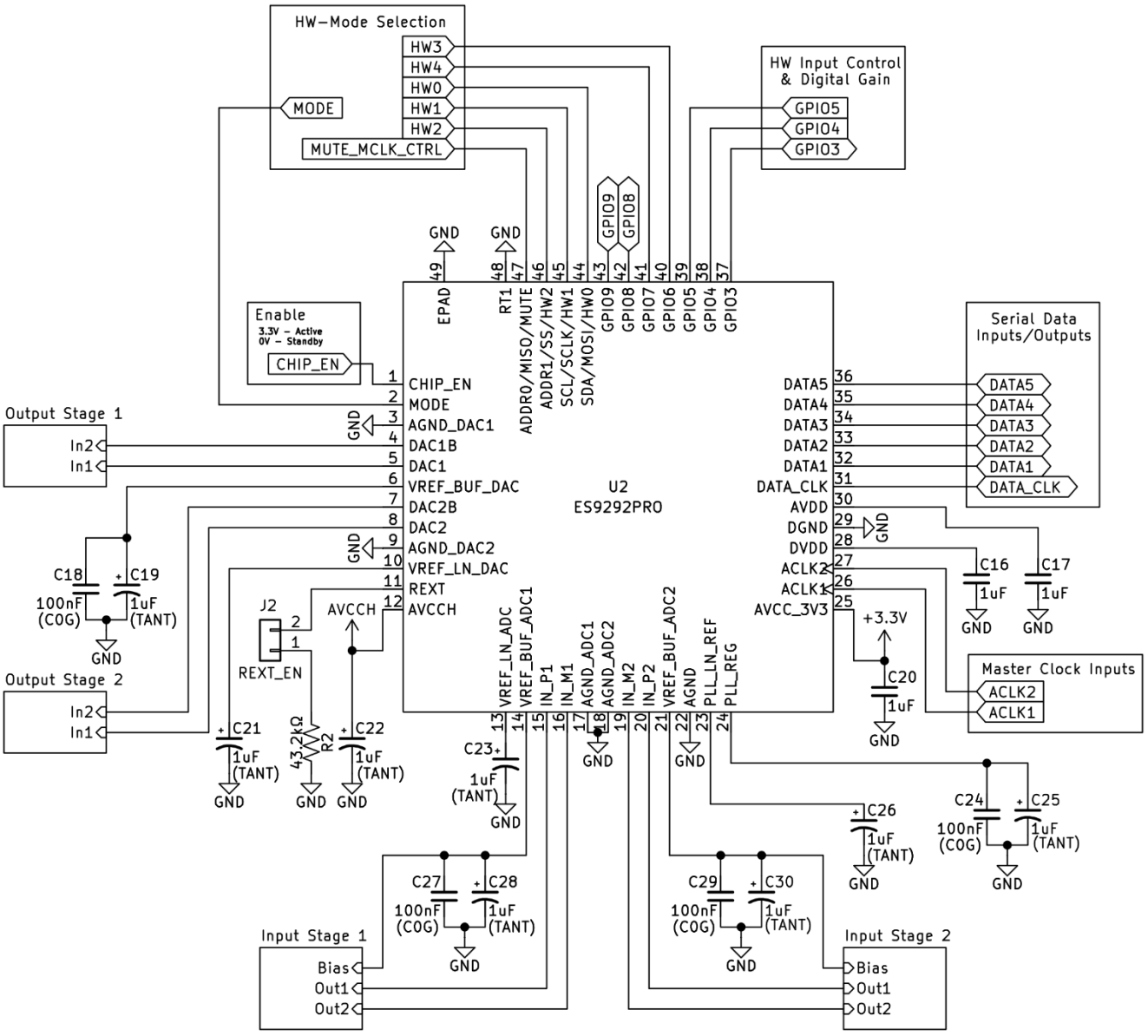


Figure 37 - ES9292PRO Hardware Mode Reference Schematic

Note 1: The ES9292PRO 48QFN package has an exposed pad (Pin 49) that must be connected to ground.

Note 2: It is recommended to use decoupling capacitors with the lowest ESR (Equivalent Series Resistance) available.

Note 3: It is recommended to use Tantalum and COG capacitors (where indicated) to achieve the highest performance.

Software (SW) Mode

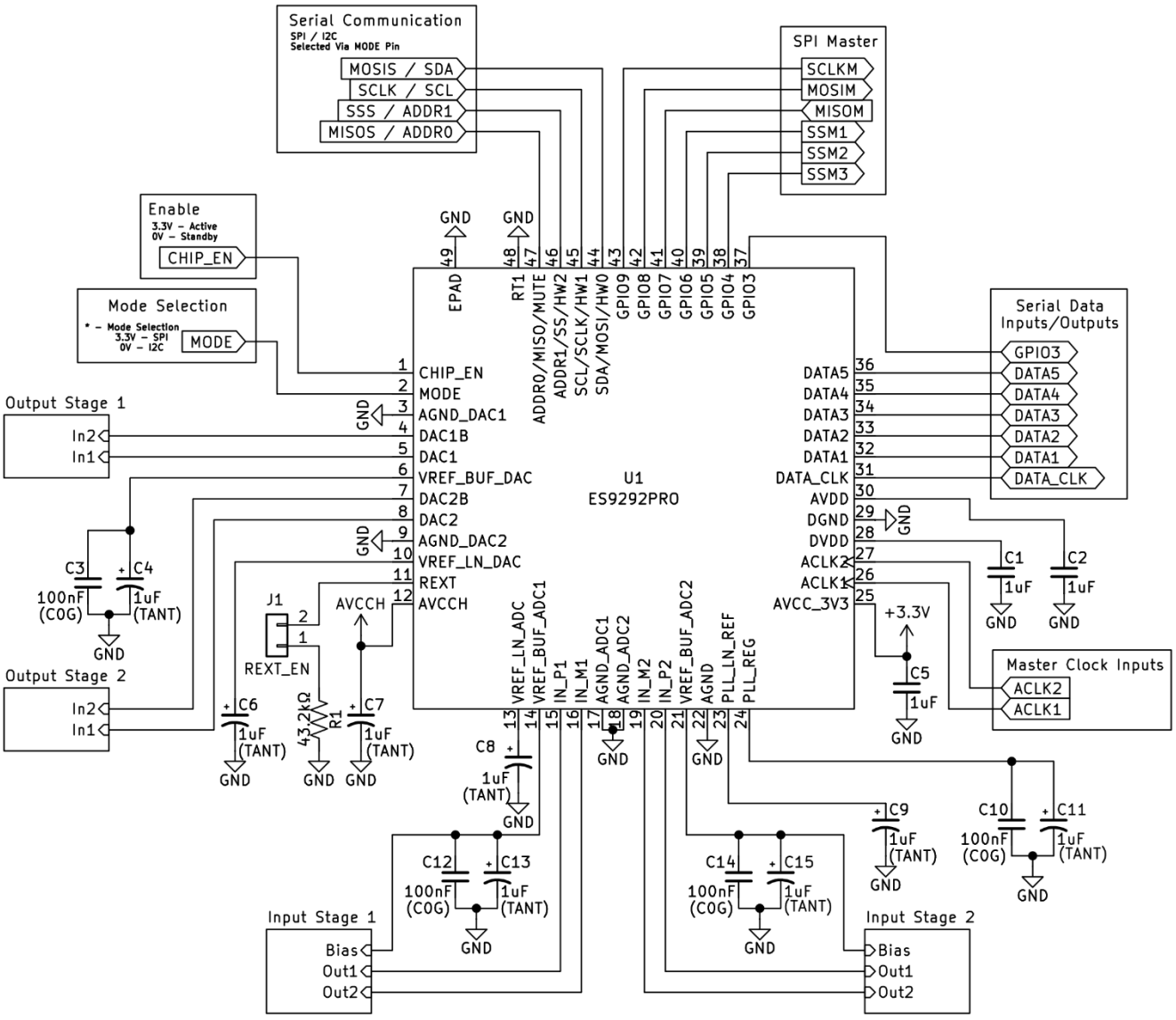


Figure 38 - ES9292PRO Software Mode Reference Schematic

Note 1: The ES9292PRO 48QFN package has an exposed pad (Pin 49) that must be connected to ground.

Note 2: It is recommended to use decoupling capacitors with the lowest ESR (Equivalent Series Resistance) available.

Note 3: It is recommended to use Tantalum and COG capacitors (where indicated) to achieve the highest performance.

Differential Input Stage (AVCCH @ 3.3V)

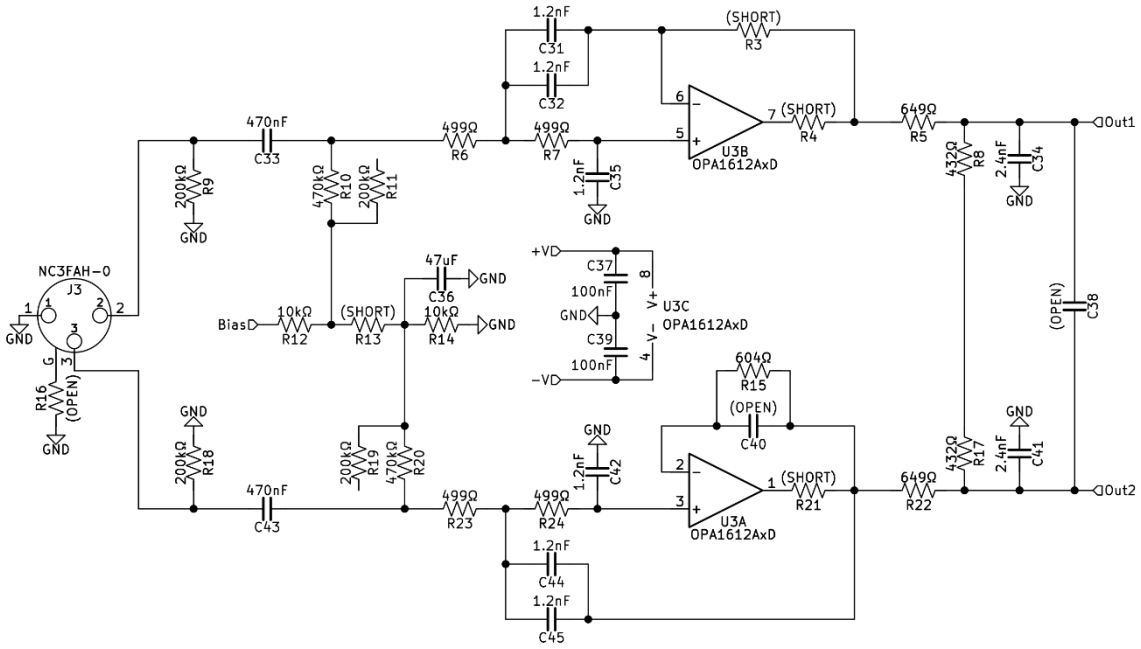


Figure 39 - ES9292PRO Differential Input Stage Reference Schematic (AVCCH @ 3.3V)

Differential Input Stage (AVCCH @ 4.5V)

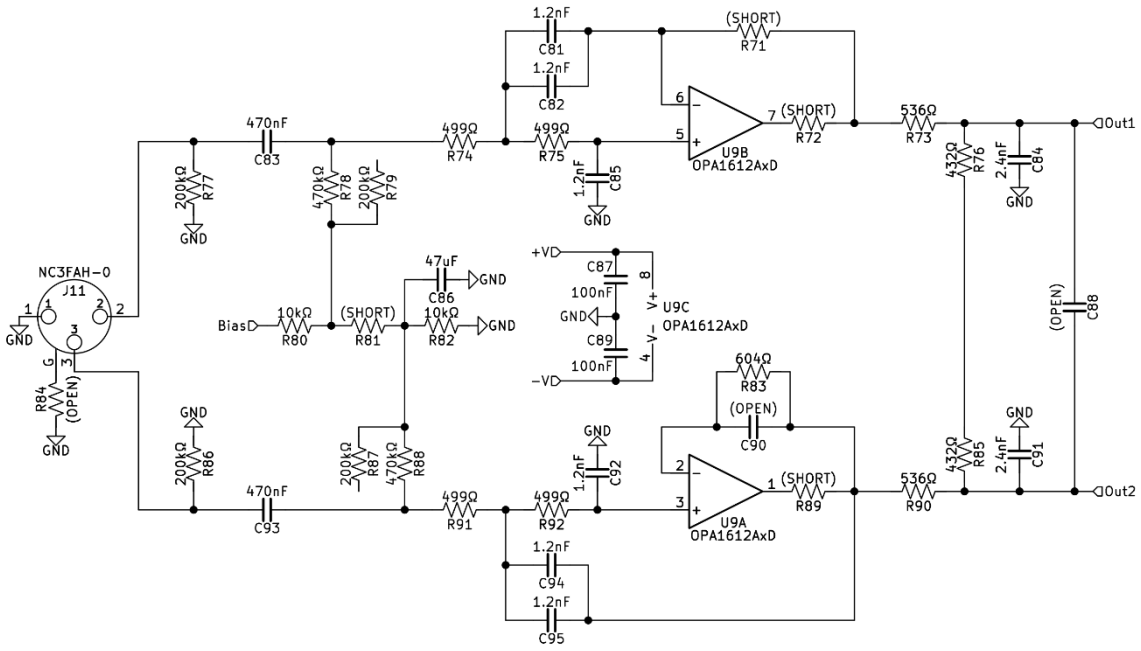


Figure 40 - ES9292PRO Differential Input Stage Reference Schematic (AVCCH @ 4.5V)

Single-Ended Input Stage (AVCCH @ 3.3V)

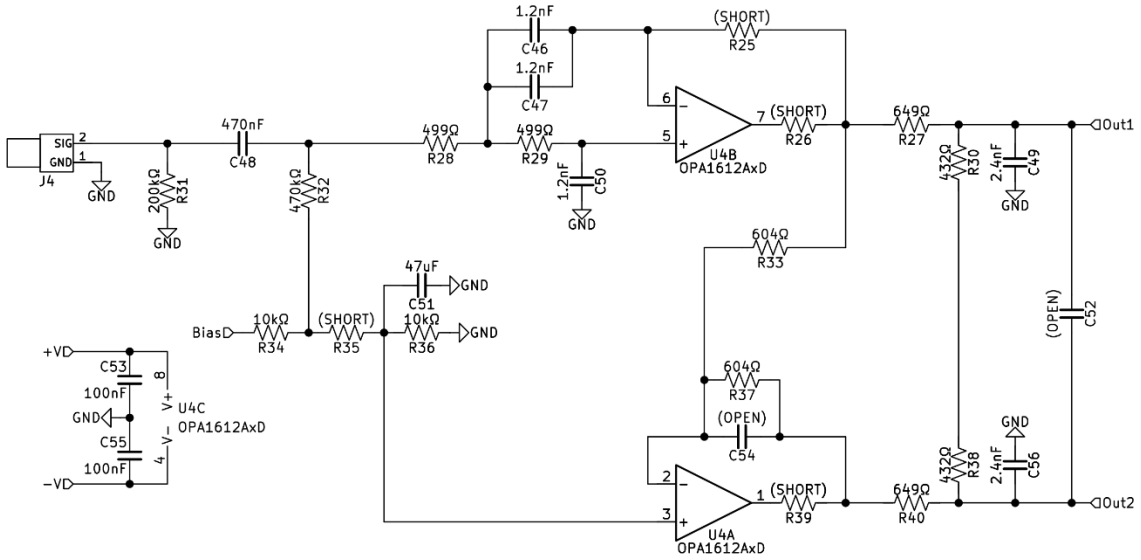


Figure 41 - ES9292PRO Single-Ended Input Stage Reference Schematic (AVCCH @ 3.3V)

Single-Ended Input Stage (AVCCH @ 4.5V)

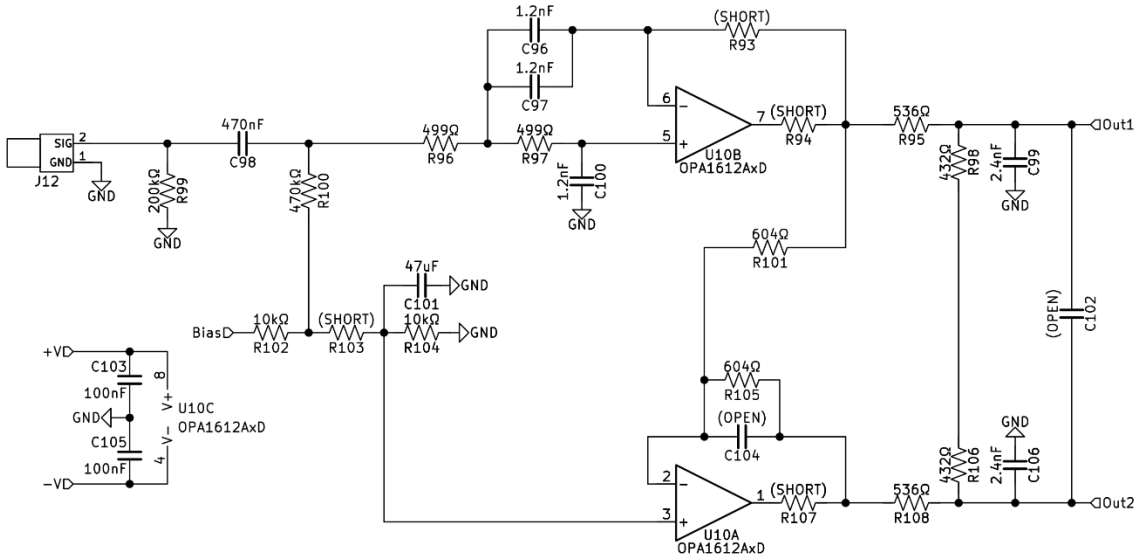


Figure 42 - ES9292PRO Single-Ended Input Stage Reference Schematic (AVCCH @ 4.5V)

Output Stage (AVCCH @ 3.3V)

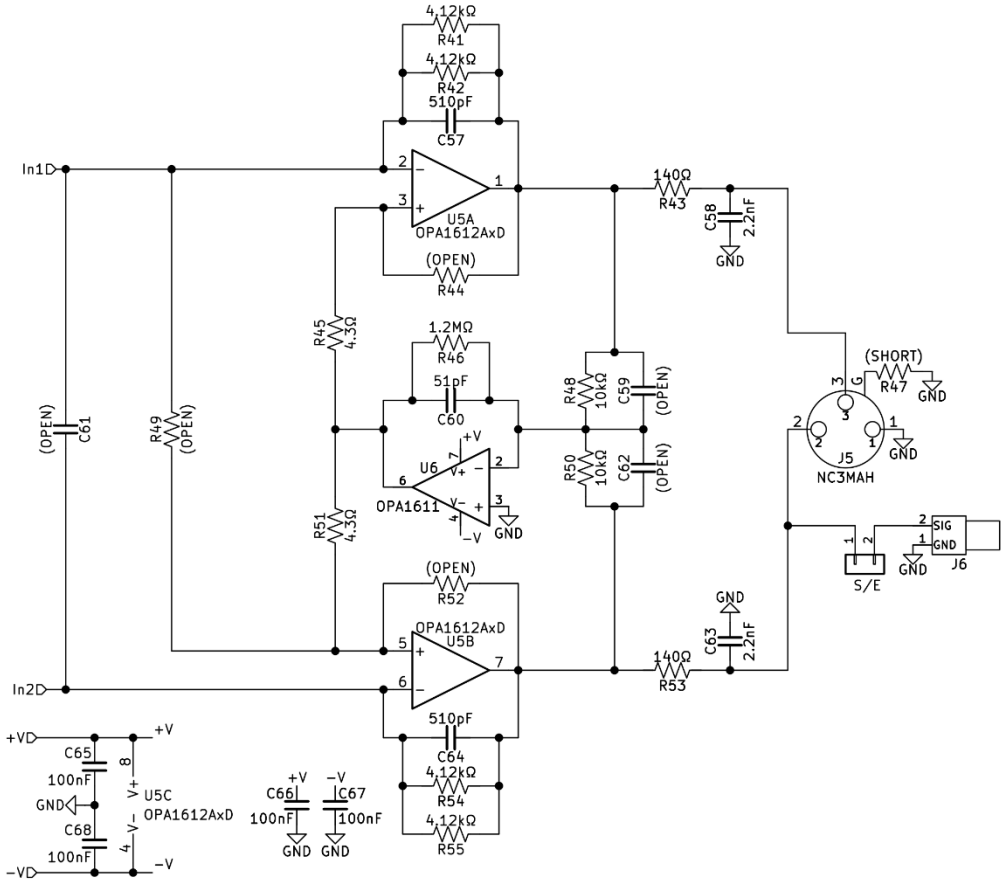


Figure 43 - ES9292PRO Output Stage Reference Schematic (AVCCH @ 3.3V)

Output Stage (AVCCH @ 4.5V)

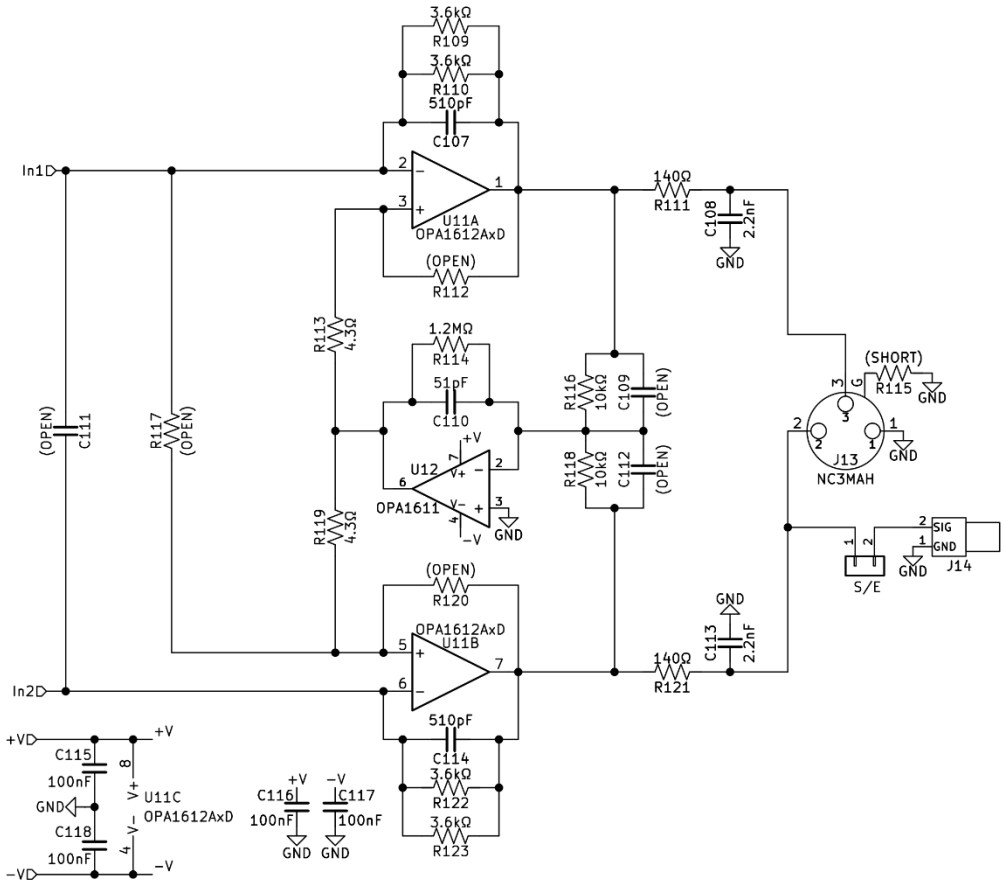


Figure 44 - ES9292PRO Output Stage Reference Schematic (AVCCH @ 4.5V)

ES9292PRO PCB Layout Guidelines

To maximize performance of the ES9292PRO ESS Technology makes the following PCB Layout recommendations:

1. Use of a 4+ layer PCB with an uninterrupted ground plane immediately beneath the chip. Both analog and digital ground signal can be connected here.
2. All bypass capacitors to be placed as close to the chip as possible while keeping clear ground paths between them and the chip's ground pins.
3. The use of multiple vias for each supply near its bypass capacitor and chip ground pin.
4. Minimize the use of vias for high-speed data and clock lines and avoid routing them near or directly underneath the analog output signals.
5. Ensure the package pad is connected to ground plane on the back side of the PCB with multiple vias for heat dissipation.

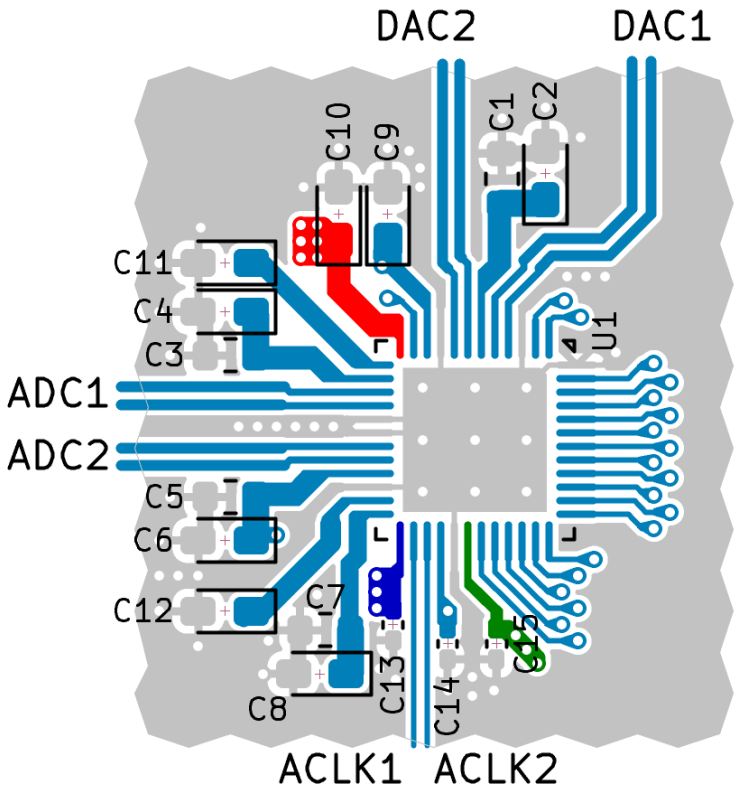


Figure 45 - ES9292PRO Recommended PCB Layout Guidelines

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2-Pb-Free Process - Classification Temperatures (Tc)). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

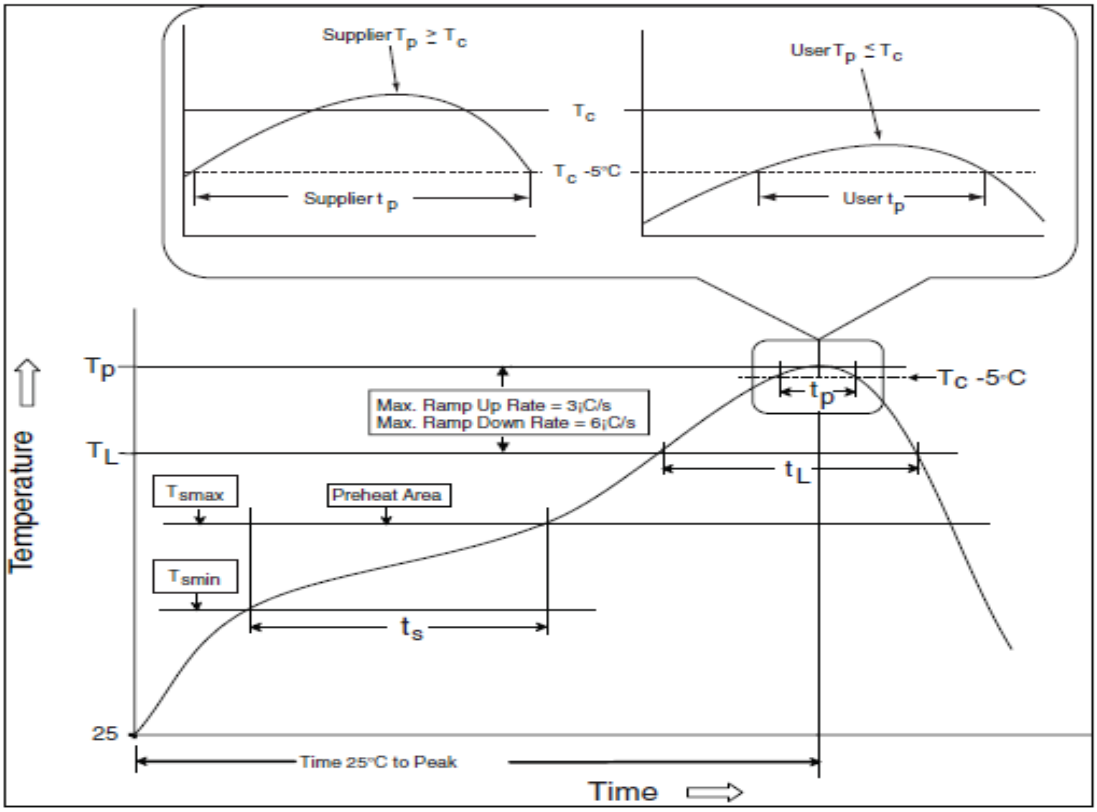


Figure 46 - IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time, bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350ºC no longer than 3 seconds.

RPC-1 Classification Reflow Profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc)	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 47 - RPC-1 Classification Reflow Profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

RPC-2 Pb-Free Process - Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 48 - RPC-2 Pb Free Classification Temperatures

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9292QPRO	SABRE 32-bit 2 Channel Ultra-High Performance CODEC with ASP2	7mm x 7mm 48 QFN

Table 49 - Ordering Information

Revision History

Current Version 0.1

Rev.	Date	Notes
0.1	August, 2026	Initial release